NCP6925

7-Channel PMIC with 2 DC-DC Converters, 5 LDOs and a Triple Input 10 Bits ADC

The NCP6925 integrated circuit is part of the ON Semiconductor mini power management IC family (PMIC). It is optimized to supply battery powered portable application sub−systems such as camera function, microprocessors. This device integrates 2 high efficiency 1 A step−down DC−DC converters, 5 low dropout (LDO) voltage regulators and a triple input 10 bits ADC in a WLCSP36 2.36 x 2.36 mm package.

Features

- 2 DC−DC Converters (3 MHz, 1 − 2.2 μH / 10 μF, 1 A)
  - Peak Efficiency 95%
  - Programmable Output Voltage from 0.6 V to 3.3 V by 12.5 mV Steps
- 5 Low Noise − Low Drop Out Regulators (2.2 μF, 300 mA)
  - Programmable Output Voltage from 0.8 V to 3.5 V by 25 mV Steps
  - 50 μVrms Typical Low Output Noise
- Triple Input 10 Bits ADC
  - Dual Resistor Measurement Mode
  - General Purpose Mode
- Control
  - Fully Programmable through a 400 kHz / 3.4 MHz I^{2}C with Pin Selectable I^{2}C Address and Interrupt Output
  - General Purpose I/O Pins that can be Used as Internal / External Regulator Enable Pins or Internal Sequences Triggered Input
  - Flexible Power−up and Down Sequences Programmable by I^{2}C
- 140 μA Very Low Quiescent Current at No Load
- Small Footprint: 2.36 x 2.36 mm WLCSP 0.4 mm Pitch

Typical Applications

- Cellular Phones, Tablets
- Digital Cameras

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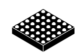


WLCSP36
FC SUFFIX
CASE 567GW

MARKING DIAGRAM

6925A
AWLYWW
▪

6925A	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Pb−Free indicator, "G" or microdot " ▪", may or may not be present.)

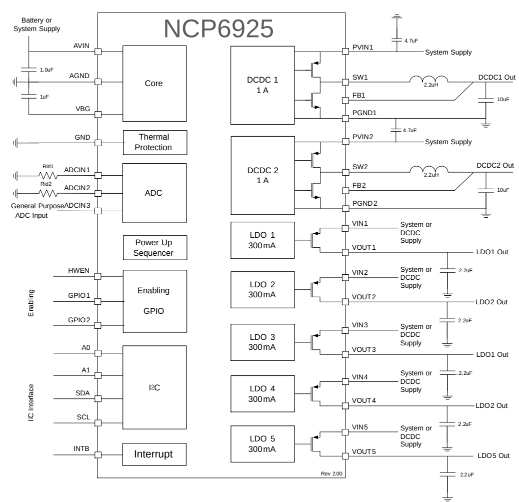


Figure 1. Application Schematic

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 42 of this data sheet.

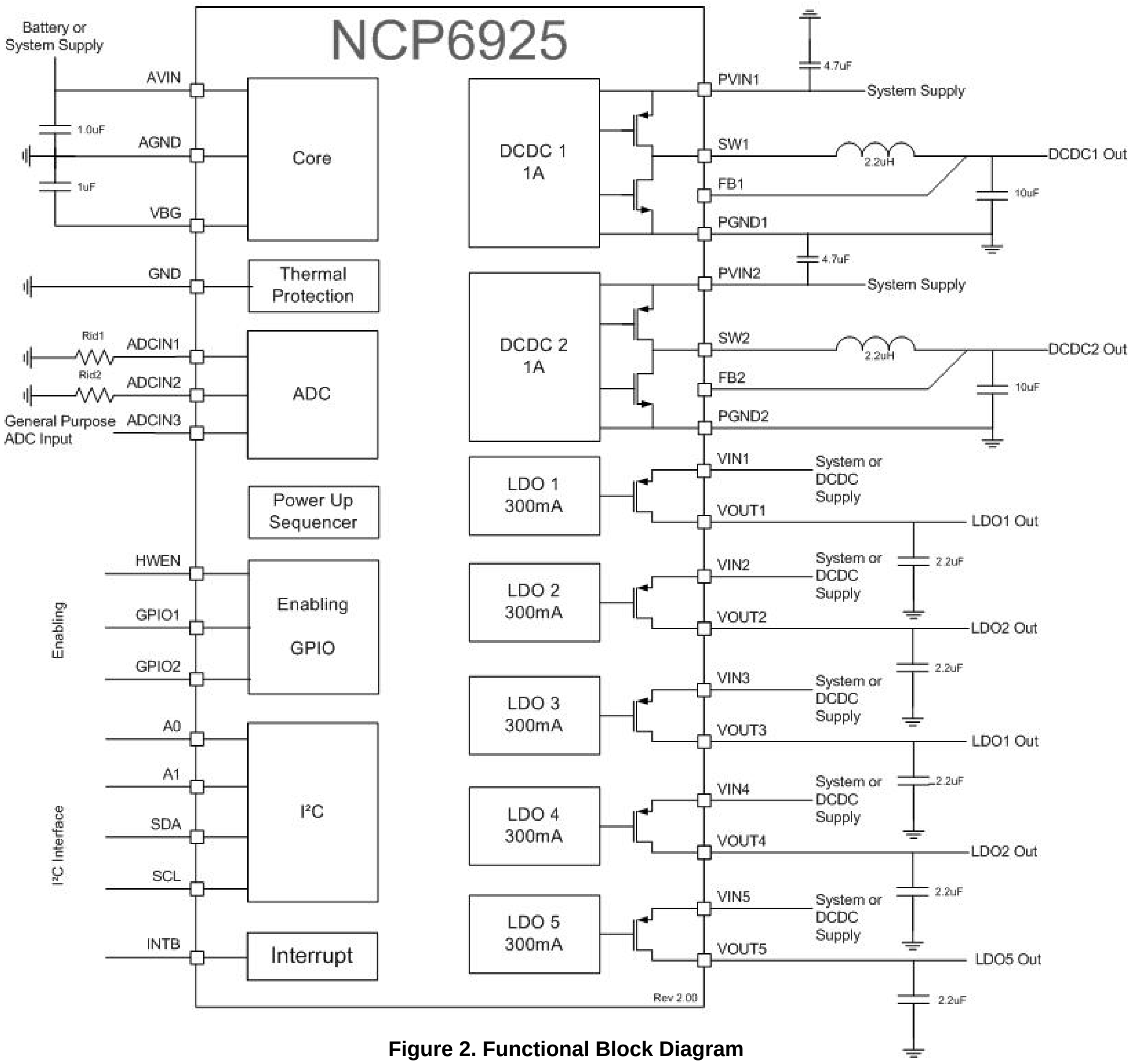


Figure 2. Functional Block Diagram

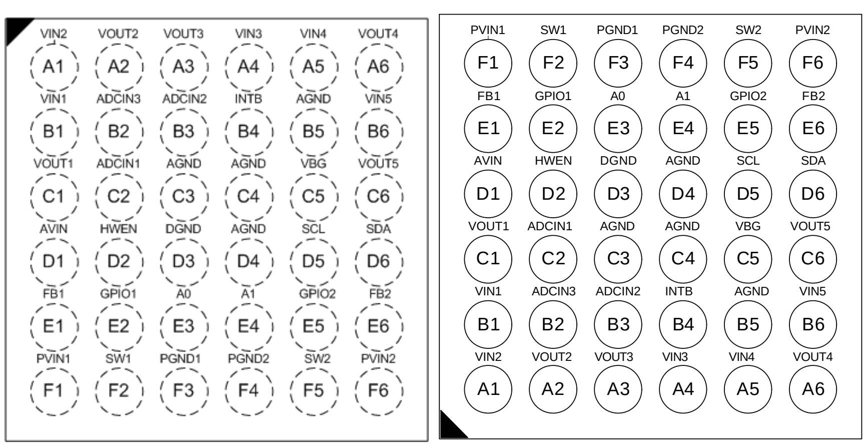


Figure 3. Pin Out Description (Top and Bottom Views)

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
SUPPLY			
D1	AVIN	Analog Input	Analog Supply. This pin is the device analog and digital supply. A 1.0 μF ceramic capacitor or larger must bypass this input to ground. This capacitor should be placed as close as possible to this pin.
B5, C3, C4, D4	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
D3	DGND	Digital Ground	Digital Ground. Analog and digital modules ground. Must be connected to the system ground.
C5	VBG	Analog Output	Reference voltage for analog internal block. This pin requires a 100 nF up to 1 μF decoupling capacitor.
CONTROL AND SERIAL INTERFACE			
D2	HWEN	Digital Input	Hardware Enable. Active high will enable the part. There is an internal pull down resistor on this pin.
D5	SCL	Digital Input	I^2C interface Clock line
D6	SDA	Digital Input/Output	I^2C interface Bi−directional Data line.
B4	INTB	Digital Output	Interrupt open drain output
E3	A0	Digital Input	I^2C selection input
E4	A1	Digital Input	I^2C selection input
E2	GPIO1	Digital Input/Output	General purpose input / output
E5	GPIO2	Digital Input/Output	General purpose input / output
DCDC CONVERTERS			
F1	PVIN1	Power Input	DCDC1 Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
F2	SW1	Power Output	DCDC1 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 − 2.2 μH inductor; refer to application section for more information.
E1	FB1	Analog Input	DCDC1 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
F3	PGND1	Power Ground	DCDC1 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
F6	PVIN2	Power Input	DCDC2 Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
F5	SW2	Power Output	DCDC2 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 − 2.2 μH inductor; refer to application section for more information.
E6	FB2	Analog Input	DCDC2 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
F4	PGND2	Power Ground	DCDC1 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
LDO REGULATORS			
B1	VIN1	Power Input	LDO1 Power Supply.
C1	VOUT1	Power Output	LDO1 Output Power. This pin requires a 1 − 2.2 μF decoupling capacitor.
A1	VIN2	Power Input	LDO2 Power Supply.
A2	VOUT2	Power Output	LDO2 Output Power. This pin requires a 1 − 2.2 μF decoupling capacitor.
A4	VIN3	Power Input	LDO3 Power Supply
A3	VOUT3	Power Output	LDO3 Output Power. This pin requires a 1 − 2.2 μF decoupling capacitor.
A5	VIN4	Power Input	LDO4 Power Supply

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
LDO REGULATORS			
A6	VOUT4	Power Output	LDO4 Output Power. This pin requires a 1 − 2.2 μF decoupling capacitor.
B6	VIN5	Power Input	LDO5 Power Supply.
C6	VOUT5	Power Output	LDO5 Output Power. This pin requires a 1 − 2.2 μF decoupling capacitor.
ADC			
C2	ADCIN1	Analog Input	10 bits ADC input 1.
B3	ADCIN2	Analog Input	10 bits ADC input 2.
B2	ADCIN3	Analog Input	10 bits ADC input 3.

Table 2. MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Analog and power pins:	V_A	−0.3 to +6.0	V
Digital pins: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A +0.3 ≤ 6.0 10	 V mA
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltages are related to AGND.
2. ESDrated to the following:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±150 V per JEDEC standard: JESD22−A115.
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN}, PV_{IN}	Analog and Power Supply		2.5		5.5	V
LDO_{VIN}	LDO Input Voltage range		1.7		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		−	40	−	°C/W
P_D	Power Dissipation Rating	T_A ≤ 85°C	−	1	−	W
		T_A = 40°C	−	2.1	−	W
L	Inductor for DC to DC converters		−	1 – 2.2	−	μH
Co	Output Capacitor for DC to DC Converters		−	10	−	μF
	Output Capacitors for LDO		−	1 − 2.2	−	μF
Cin	Input Capacitor for DC to DC Converters		−	4.7	−	μF

5. Refer to the Application Information section of this data sheet for more details.
6. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
7. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a NCP6925EVB board. It is a multilayer board with 1−ounce internal power and ground planes and 2−ounce copper traces on top and bottom of the board.
8. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A = −40°C to +85°C unless otherwise specified. AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = 3.6 V (Unless otherwise noted). DCDC1 = 1.05 V, DCDC2 = 1.2 V, LDO1&2&3 = 2.85 V, LDO4&5 = 1.8 V. Typical values are referenced to T_A = +25°C and default configuration (Note 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: Pins AV_{IN} – PV_{IN1} – PV_{IN2} – V_{IN1} – V_{IN2} – V_{IN3}– V_{IN4} – V_{IN5}						
I_Q	Operating quiescent current	DCDC1&2 on, no load, no switching LDOs off	−	65	−	μA
		DCDC1&2 on, no load, no switching LDOs on, no load T_A = up to +85°C	−	140	−	
		DCDC1&2 Off LDOs on, no load T_A = up to +85 °C	−	45	−	
I_{SLEEP}	Sleep mode current	HWEN pin on All DC to DC and LDOs off V_{IN} = 2.5 V to 5.5 V T_A = up to +85°C	−	7.5	−	μA
I_{OFF}	Shutdown current	All DCDCs and LDOs off HWEN pin = off I^2C interface disabled V_{IN} = 2.5 V to 5.5 V	−	0.3	2	μA
DCDC1&2 STEP DOWN CONVERTERS						
PV_{IN}	Input Voltage Range		2.5	−	5.5	V
	Output Voltage Range		0.600	−	3.3	V
	Programming Granularity		−	12.5	−	mV
I_{OUTMAX}	Maximum Output Current		1	−	−	A
ΔV_{OUT}	Output Voltage DC Error	I_{OUT} = 300 mA	−1	0	1	%
F_{SW}	Switching Frequency		2.7	−	3.3	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PVIN pins to SW pins PV_{IN} = 3.6 V	−	180	−	mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW pins to PGND pins PV_{IN} = 3.6 V	−	78	−	mΩ
I_{PK}	Peak Inductor Current	2.5 V ≤ PV_{IN} ≤ 5.5 V	1.3	1.6	1.9	A
	Load Regulation	I_{OUT} from 300 mA to I_{OUTMAX}	−	5	−	mV/A
	Line Regulation	I_{OUT} = 300mA 2.5 V ≤ PV_{IN} ≤ 5.5V	−	0	−	mV
D	Maximum Duty Cycle		−	100	−	%
t_{START}	Soft−Start Time		−	850	−	μs
$R_{DISDCDC}$	DCDC Active Output Discharge		−	7	−	Ω
U_{VP_BUCK}	Under voltage threshold detection		−	V_{OUT_BUCK} x 0.9	−	V
LDO1 TO LDO5 LOW DROP OUT REGULATORS						
V_{IN}	Input voltage range		1.7	−	5.5	V
V_{OUT}	Output Voltage Range		0.8	−	3.50	V
	Programming Granularity		−	25	−	mV
I_{OUTMAX}	Maximum Output Current		300	−	−	mA
I_{LIM}	Current limitation	(Note 11)	360	−	700	mA
I_{SC}	Short Circuit Protection	Foldback current	−	180	−	mA

9. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
10. Refer to the Application Information section of this data sheet for more details.
11. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A = −40°C to +85°C unless otherwise specified. AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = 3.6 V (Unless otherwise noted). DCDC1 = 1.05 V, DCDC2 = 1.2 V, LDO1&2&3 = 2.85 V, LDO4&5 = 1.8 V. Typical values are referenced to T_A = +25°C and default configuration (Note 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO1 TO LDO5 LOW DROP OUT REGULATORS						
t_{START}	Soft−Start Time	Vout = 1.8 V Vout = 2.85 V	− −	110 160	− −	μs
ΔV_{OUT}	Output Voltage Accuracy DC	I_{OUT} = 300 mA	−2	V_{NOM}	+2	%
	Load Regulation	I_{OUT} = 0 mA to 300 mA	−	0.4	−	%
	Line Regulation	V_{IN} = 2.5 V to 5.5 V V_{OUT} = 1.8 V, I_{OUT} = 300 mA	−	0.3	−	%
V_{DROP}	Dropout Voltage	I_{OUT} = 300 mA V_{OUT} = V_{NOM} – 2%, V_{NOM} = 1.8 V V_{OUT} = V_{NOM} – 2%, V_{NOM} = 2.85 V	 − −	 300 170	 − −	mV
PSRR	Ripple Rejection	F = 10 kHz V_{OUT} = 2.8 V, I_{OUT} = 100 mA (Note 11)	−	−50	−	dB
Noise		100 Hz → 100 kHz, V_{OUT} = 2.8 V, I_{OUT} = 100 mA (Note 11)	−	50	−	μV
R_{DISLDO}	LDO Active Output Discharge		−	25	−	Ω
U_{VP_LDO}	Under voltage threshold detection		−	V_{OUT_LDO} x 0.875	−	V
ADC						
	Reference voltage	Bandgap x 2	−	2.4	−	V
	Input Range	From zero to full scale	0	−	2.390	V
	Resolution		−	2.344	−	mV
	Offset error		−1	−	+1	LSB
	Gain error	% of the FS	−	±0.5	−	%
	INL	Integral non−linearity	−1.5	−	+1.5	LSB
	DNL	Differential non−linearity	−1.5	−	+1.5	LSB
HWEN, A0, A1						
V_{IH}	Positive Going Input High Voltage Threshold		1.1	−	−	V
V_{IL}	Negative Going Input Low Voltage Threshold		−	−	0.4	V
I_{PD}	Pull−Down (input bias current)		−	0.1	1.0	μA
GPIO1, GPIO2						
V_{IH}	Positive Going Input High Voltage Threshold		1.1	−	−	V
V_{IL}	Negative Going Input Low Voltage Threshold		−	−	0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = −1 mA	AV_{IN} – 0.45	−	−	V
V_{OL}	Low Level Output Voltage	I_{OH} = 1 mA	−	−	0.45	V
I^2C						
V_{I2CINT}	High level at SCL/SDA line	(Note 11)	−	−	5.0	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Note 11)	−	−	0.5	V

9. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
10. Refer to the Application Information section of this data sheet for more details.
11. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A = −40°C to +85°C unless otherwise specified. AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = 3.6 V (Unless otherwise noted). DCDC1 = 1.05 V, DCDC2 = 1.2 V, LDO1&2&3 = 2.85 V, LDO4&5 = 1.8 V. Typical values are referenced to T_A = +25°C and default configuration (Note 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I^2C						
V_{I2CIH}	SCL, SDA high input voltage	SCL, SDA pin (Note 11)	0.8 x V_{I2CINT}	−	−	V
V_{I2COL}	SCL, SDA low output voltage	I_{SINK} = 3 mA (Note 11)	−	−	0.4	V
F_{SCL}	I^2C clock frequency	(Note 11)	−	−	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	−	−	2.3	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	130	200	mV
T_{dlysys}	Initialization time at power on		−	2	−	ms
T_{SD}	Thermal Shut Down Protection	(Note 11)	−	150	−	°C
$T_{WARNING}$	Warning Rising Edge	(Note 11)	−	135	−	°C
T_{SDHYS}	Thermal Shut Down Hysteresis	(Note 11)	−	35	−	°C

9. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
10. Refer to the Application Information section of this data sheet for more details.
11. Guaranteed by design and characterized.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{INLDOx}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 2.2 μH (DFE201612R−H−2R2N) − C_{DCDC} = 10 μF 0603.

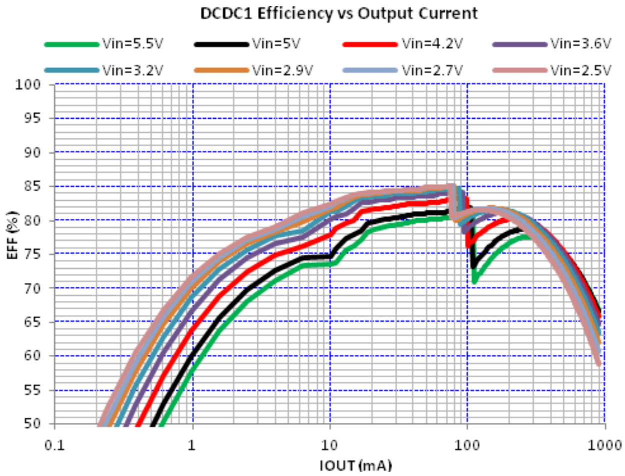


Figure 4. DCDC1 Efficiency vs. IOUT (auto mode) VOUT = 0.6 V

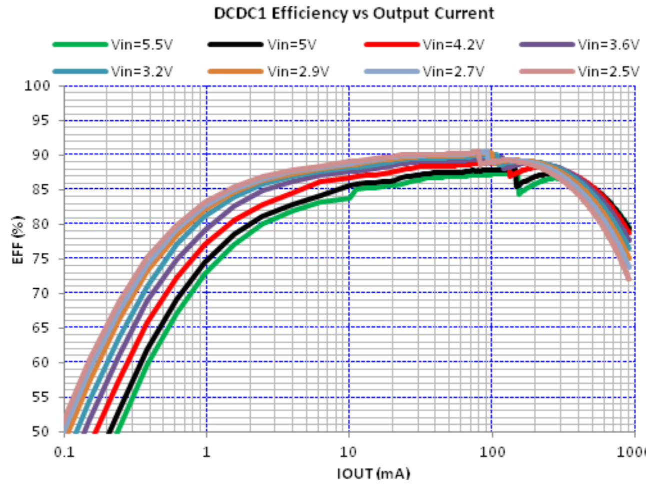


Figure 5. DCDC1 Efficiency vs. IOUT (auto mode) VOUT = 1.2 V

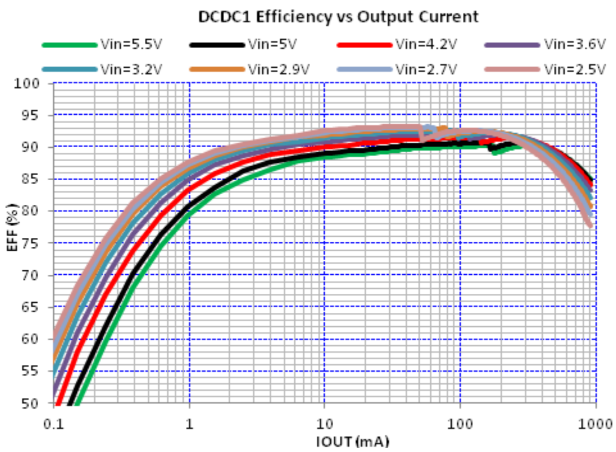


Figure 6. DCDC1 Efficiency vs. IOUT (auto mode) VOUT = 1.8 V

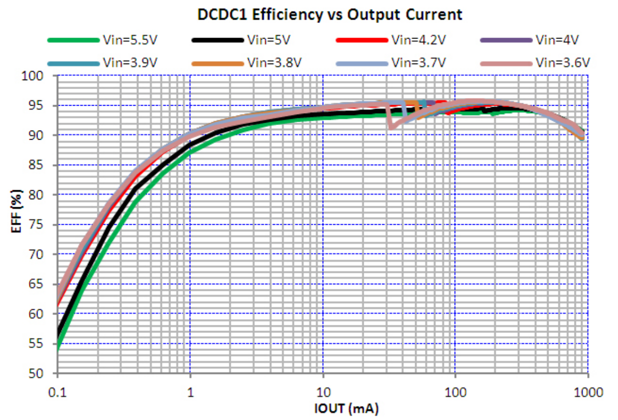


Figure 7. DCDC1 Efficiency vs. IOUT (auto mode) VOUT = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{INLDOx}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 2.2 μH (DFE201612R−H−2R2N) − C_{DCDC} = 10 μF 0603.

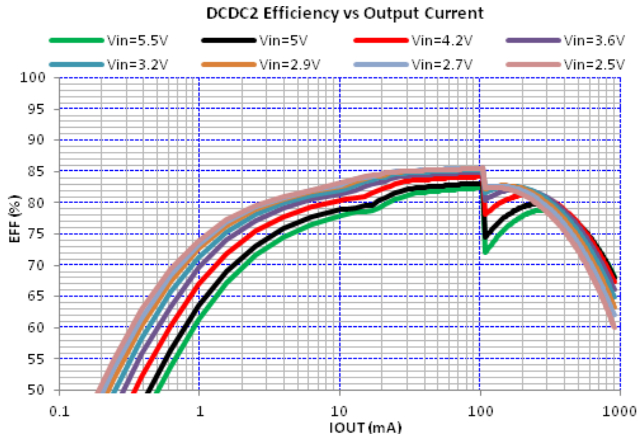


Figure 8. DCDC2 Efficiency vs. IOUT (auto mode) VOUT = 0.6 V

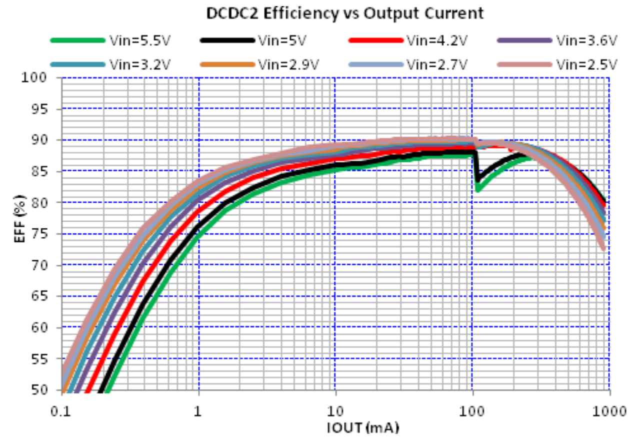


Figure 9. DCDC2 Efficiency vs. IOUT (auto mode) VOUT = 1.2 V

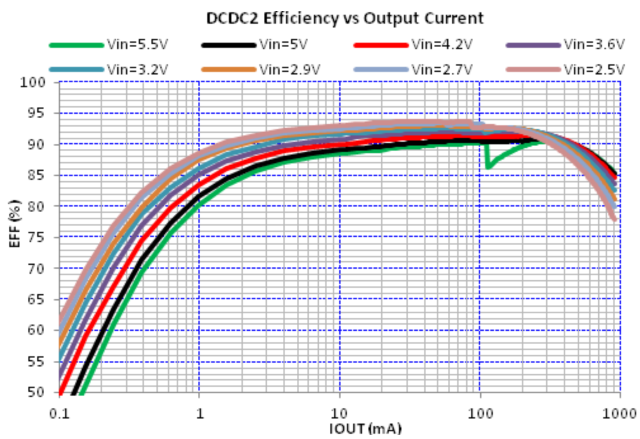


Figure 10. DCDC2 Efficiency vs. IOUT (auto mode) VOUT = 1.8 V

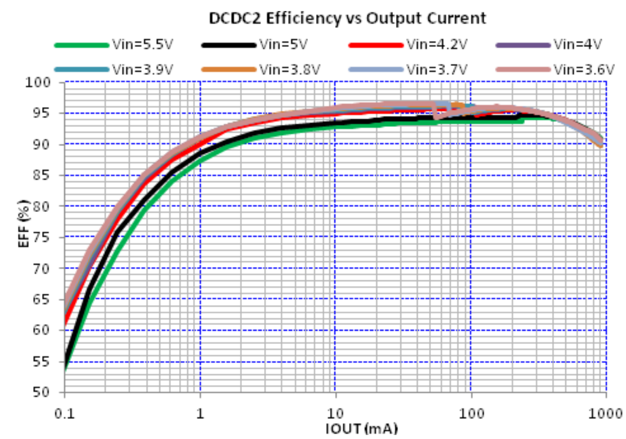


Figure 11. DCDC2 Efficiency vs. IOUT (auto mode) VOUT = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{INLDOx}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 µF 0603, L_{DCDC} = 2.2 µH (DFE201612R−H−2R2N) − C_{DCDC} = 10 µF 0603.

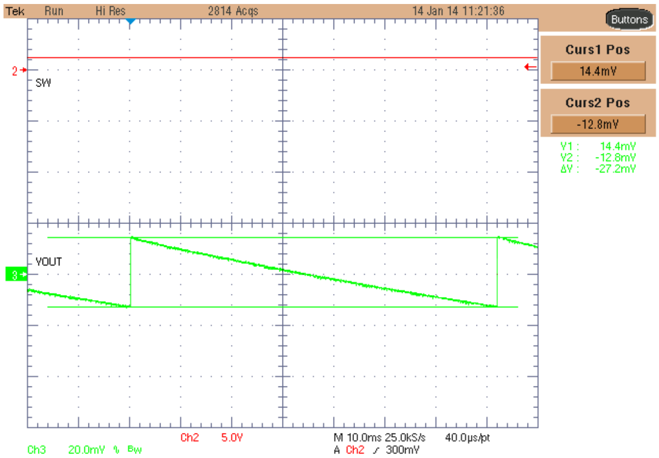


Figure 12. DCDC1 Ripple Voltage in PFM Mode (V_{IN} = 3.6V – V_{OUT} = 1.2 V – No load)

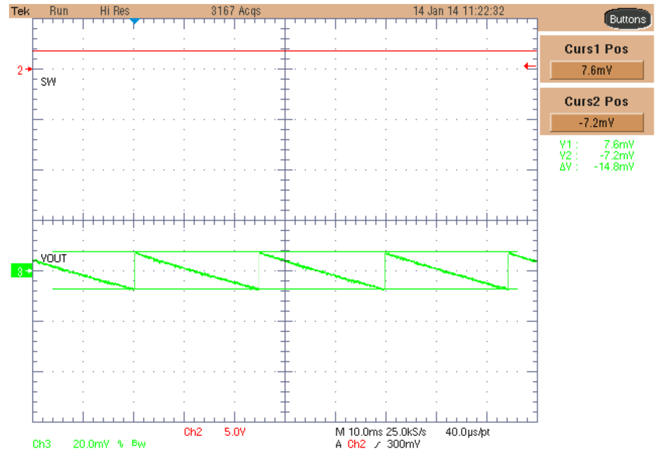


Figure 13. DCDC1 Ripple Voltage in PFM Mode (V_{IN} = 3.6 V – V_{OUT} = 1.8 V – No load)

Figure 14. DCDC2 Ripple Voltage in PFM Mode (V_{IN} = 3.6 V – V_{OUT} = 1.2 V – No load)

Figure 15. DCDC2 Ripple Voltage in PFM Mode (V_{IN} = 3.6 V – V_{OUT} = 1.8 V – No load)

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{INLDOx}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 µF 0603, L_{DCDC} = 2.2 µH (DFE201612R−H−2R2N) − C_{DCDC} = 10 µF 0603.

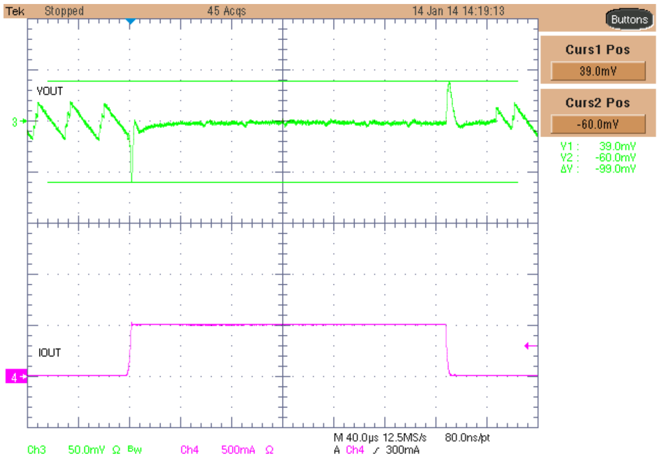


Figure 16. DCDC1 Load Transient Response (PWM Mode, V_{IN} = 3.6 V – V_{OUT} = 1.2 V)

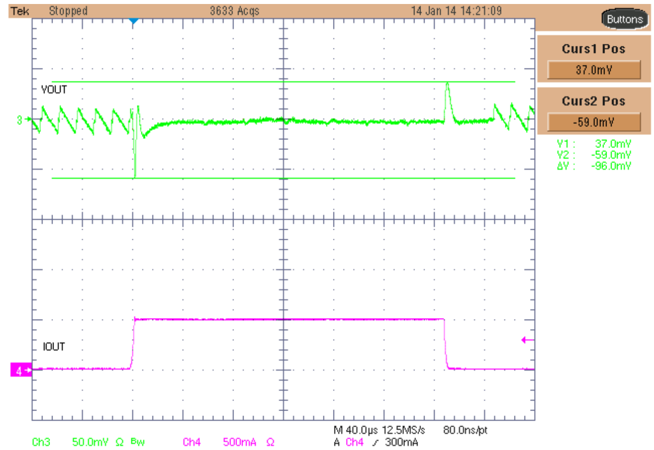


Figure 17. DCDC1 Load Transient Response (PWM Mode, V_{IN} = 3.6 V – V_{OUT} = 1.8 V)

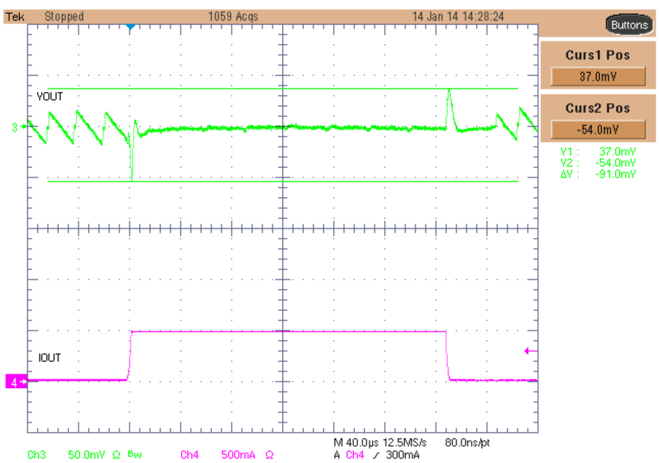


Figure 18. DCDC2 Load Transient Response (PWM Mode, V_{IN} = 3.6 V – V_{OUT} = 1.2 V)

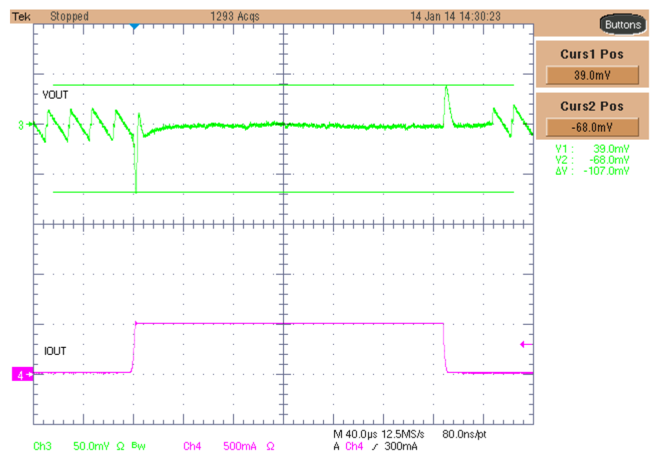


Figure 19. DCDC2 Load Transient Response (PWM Mode, V_{IN} = 3.6 V – V_{OUT} = 1.8 V)

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{INLDOx}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 2.2 μH (DFE201612R−H−2R2N) − C_{DCDC} = 10 μF 0603.

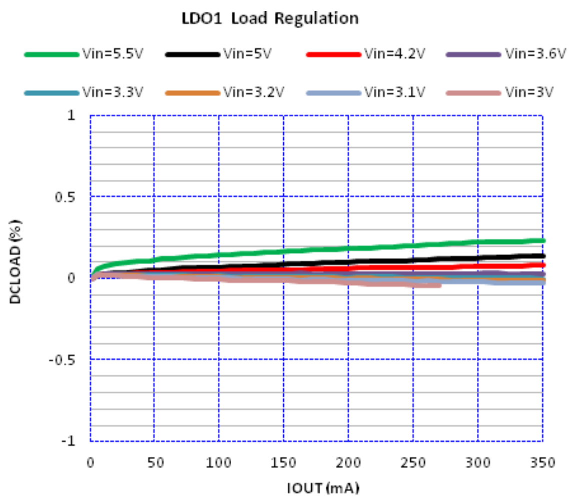


Figure 20. LDO1 Load Regulation (V_{OUT} = 2.8 V)

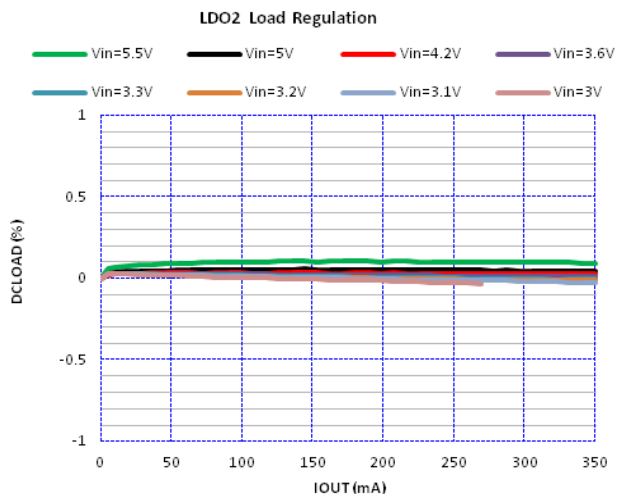


Figure 21. LDO2 Load Regulation (V_{OUT} = 2.8 V)

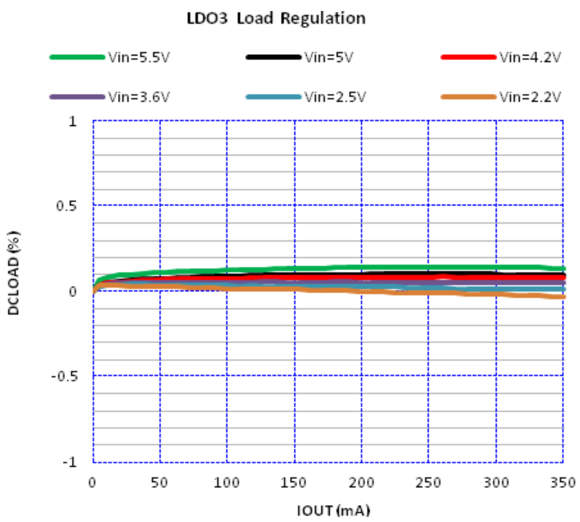


Figure 22. LDO3 Load Regulation (V_{OUT} = 1.8 V)

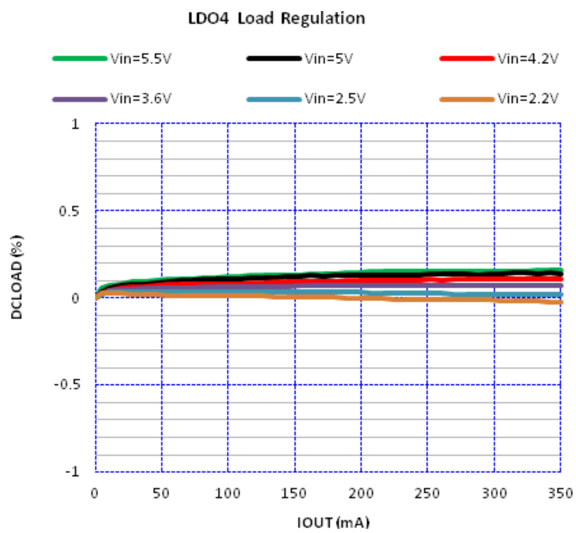


Figure 23. LDO4 Load Regulation (V_{OUT} = 1.8 V)

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{INLDOx}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 µF 0603, L_{DCDC} = 2.2 µH (DFE201612R−H−2R2N) − C_{DCDC} = 10 µF 0603.

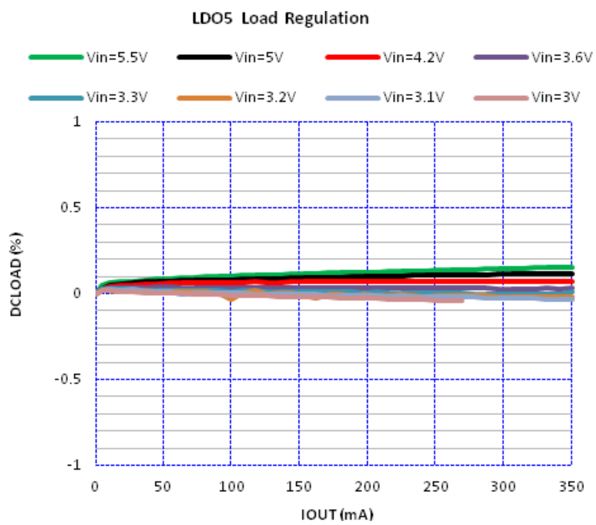


Figure 24. LDO5 Load Regulation (V_{OUT} = 2.8 V)

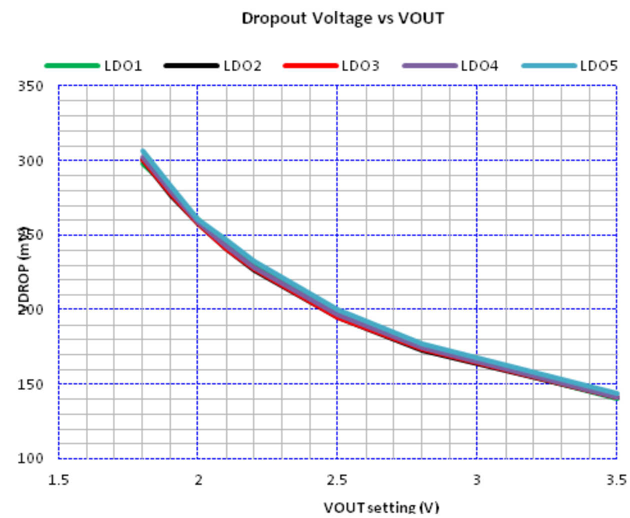


Figure 25. Dropout Voltage vs Vout (I_{OUT} = 300 mA)

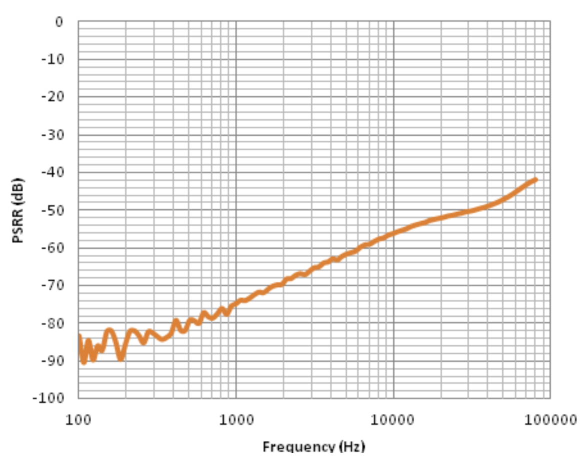


Figure 26. LDOx PSRR (V_{IN} = 3.6 V – V_{OUT} = 1.8 V – I_{OUT} = 5 mA)

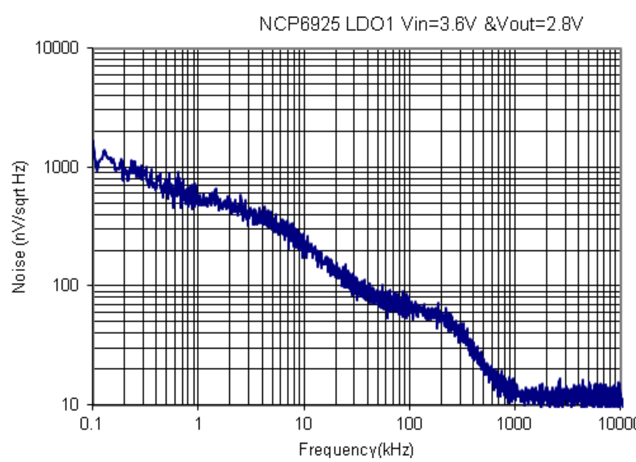


Figure 27. LDOx Output Noise (V_{IN} = 3.6 V – V_{OUT} = 2.8 V – I_{OUT} = 10 mA)

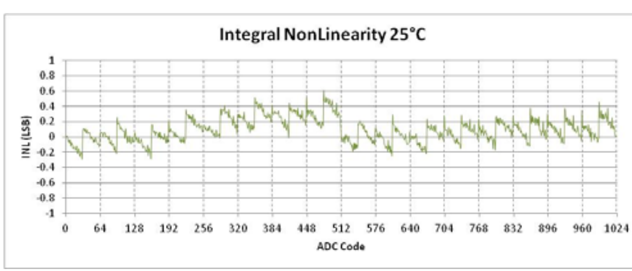


Figure 28. ADC INL

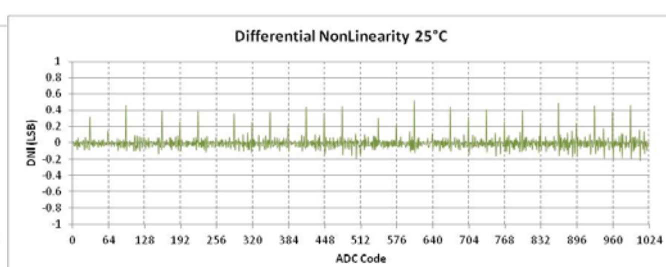


Figure 29. ADC DNL

DETAILED OPERATING DESCRIPTION

General Description

The NCP6925 mini power management integrated circuit is optimized to supply different sub systems of battery powered portable applications. The IC can be supplied directly from the latest technology single cell batteries such as Lithium−Polymer as well as from triple alkaline cells. Alternatively, the IC can be supplied from a pre−regulated supply rail in case of multi−cell or main powered applications.

It integrates two switched mode DCDC converters and five low dropout linear regulators. The IC is widely programmable through an I^2C interface and includes low level IO signaling. An analog core provides the necessary references for the IC while a digital core ensures proper control.

The output voltage range, current capabilities and performance of the switched mode DCDC converters are well suited to supply the different peripherals in the system as well as to supply processor cores. For PWM operation, the converters run on a local 3 MHz clock. A low power PFM mode is provided that ensures that even at low loads high efficiency can be obtained. All the switching components are integrated including the compensation networks and synchronous rectifier. Only a small sized 1− 2.2 μH inductor and 10 μF bypass capacitor are required for typical applications.

The general purpose low dropout regulators can be used to supply the lower power rails in the application. To improve the overall application standby current, the bias current of these regulators are made very low. The regulators have their own input supply pin to be able to connect them independently to either the system supply voltage or to the output of the DCDC converter in the application. The regulators are bypassed with a small size 1 − 2.2 μF capacitor.

The feature can be controlled through the I^2C interface. In addition to this bus, digital control pins including hardware enable (HWEN), two general purpose inputs / outputs (GPIOx) and interrupt (INTB) are provided.

The 10 bits triple input analog to digital converter checks and store the resistor value placed on ADCIN1 and ADCIN2. It is used to store the ID of the external module which help to have the right configuration for each converter.

Under Voltage Lockout

The core does not operate for voltages below the Under Voltage Lock Out (UVLO) level. Below the UVLO threshold, all internal circuitry (both analog and digital) is held in reset.

NCP6925 operation is guaranteed down to UVLO when battery voltage is dropping off. To avoid erratic on / off behaviour, a typical 130 mV hysteresis is implemented. When an UVLO event occurs and the AV_{IN} voltage recovers, NCP6925 is initialized in its default state.

Thermal Shutdown

The thermal capabilities of the device can be exceeded due to the output power capabilities of the on chip step down converters and low drop out regulators. A thermal protection circuit is therefore implemented to prevent the part from being damaged. This protection circuit is only activated when the core is in active mode (at least one output channel is enabled). During thermal shutdown, all outputs of the NCP6925 are off.

When the NCP6925 returns from thermal shutdown mode, it can re−start in three different configurations depending on REARM[1:0] bits:

- If REARM[1:0] = 00, NCP6925 re−starts with default register values,
- If REARM[1:0] = 01 NCP6925 re−starts with register values set prior to thermal shutdown,
- Finally if REARM[1:0] = 10, NCP6925 does not re−start automatically, a toggle of HWEN or CHx_EN[] or SEQx_CTRL[] is needed.

In addition, a thermal warning is implemented which can inform the processor through an interrupt (if not masked) that NCP6925 is close to its thermal shutdown so that preventive measurement can be taken by software.

Active Output Discharge

To prevent any disturbances on the power−up sequence, a quick active output discharge is done during the start−up sequence for all output channels.

When the IC is turned off through HWEN pin (or ENx bits) or AVIN drops down below UVLO threshold, no shut down sequence is expected, all supplies are disabled and outputs discharged simultaneously.

Enabling / Disabling

The HWEN pin controls the device start up without enabling the output of the converters. If HWEN is raised, this starts the internal circuitry. By default all the converters are off. If HWEN is made low, device enters in shutdown mode and all regulators are turned off. Regulators can also be turned off with the dedicated register. A built−in pull−down resistor disables the device if this pin is left unconnected.

When HWEN is high, the different power rails can be independently enabled / disabled by writing the appropriate bit in the ENABLE register.

When HWEN is low, NCP6925 is in power down mode and I^2C will return NACK to any request. After HWEN transition from low to high, initialization sequence and ADC 1&2 read will be performed. During this sequence is performed, I^2C will NACK any request too. I^2C will be accessible after sequence and ADC completion are completed.

Power Up / Down Sequence and HWEN

Power up and power down sequence can be program and controlled with the dedicated register (BUCKx_SEQ[7:0], LDO12_SEQ[7:0], LDO34_SEQ[7:0], LDO5_SEQ[3:0], CHx_SEQ[7:0], SEQ1_PROG[7:0], SEQ2_PROG[7:0]). SEQx_CTRL[1:0] set the power−up or shut down. Converters can also be turned on and off independently with the CHx_EN[6:0] register.

When a shutdown is required during a power−up, it will be valid and start when the power−up is finished.

Any changes in BUCKx_SEQ[7:0], LDO12_SEQ[7:0], LDO34_SEQ[7:0], LDO5_SEQ[3:0] during a power−up or shutdown is not valid and will not modify the NCP6925 setting.

Slot Period and DCDC Soft Start Time Setting

(details Table 35)

SEQ_SPEED[1:0] defines the slot period of the 2 sequences. The DCDC soft start time selection is linked to the slot period as the setting is also done with SEQ_SPEED[1:0].

Any changes in SEQ_SPEED[1:0] during a power−up or shut down sequence is valid only when the sequence is finished.

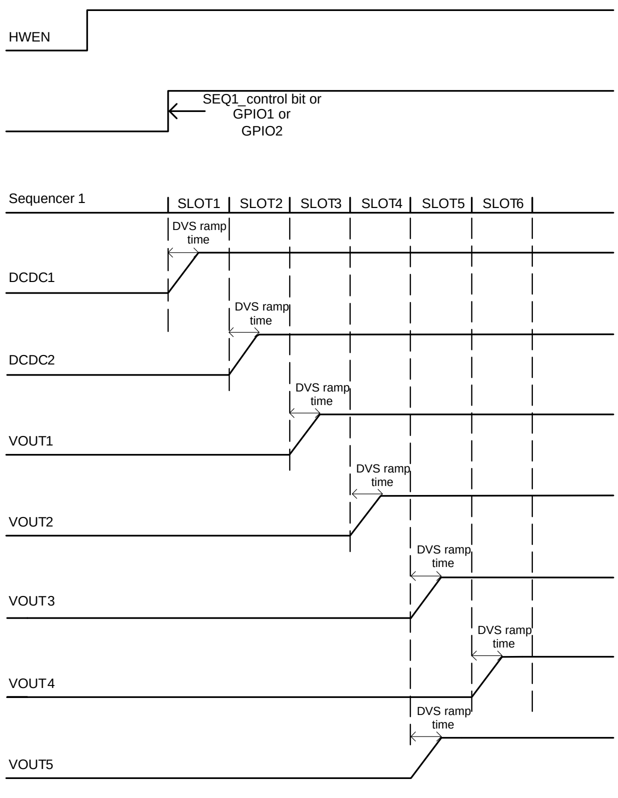


Figure 30.

Example for Sequencer 1 with DCDC1 assign to SLOT1, DCDC2 assign to SLOT2, VOUT1 assign to SLOT3, VOUT2 assign to SLOT4, VOUT3 assign to SLOT5, VOUT4 assign to SLOT6, VOUT5 assign to SLOT5

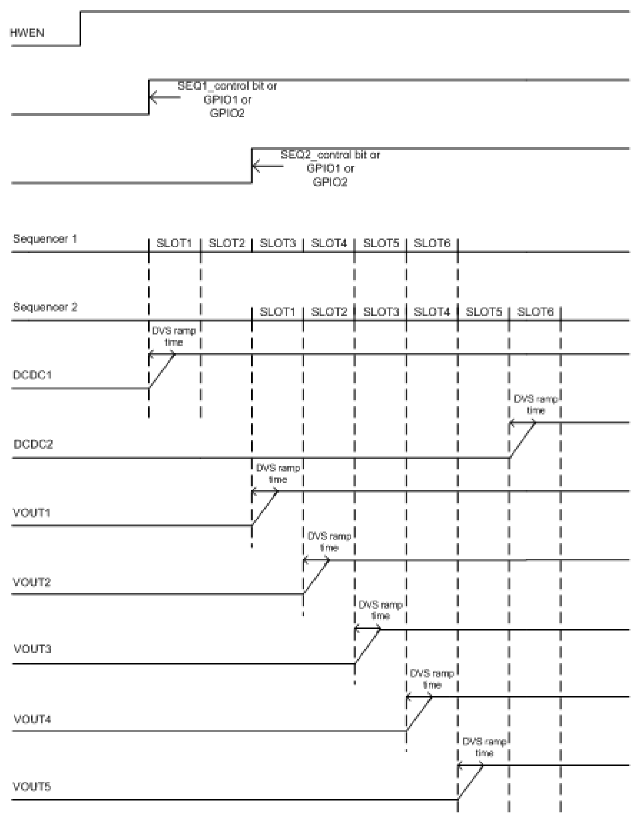


Figure 31.

Example for Sequencer 1and Sequencer 2 with DCDC1 assign to SLOT1 SEQ1, DCDC2 assign to SLOT6 SEQ2, VOUT1 assign to SLOT1 SEQ2, VOUT2 assign to SLOT2 SEQ2, VOUT3 assign to SLOT5 SEQ1, VOUT4 assign to SLOT6 SEQ1, VOUT5 assign to SLOT5 SEQ2

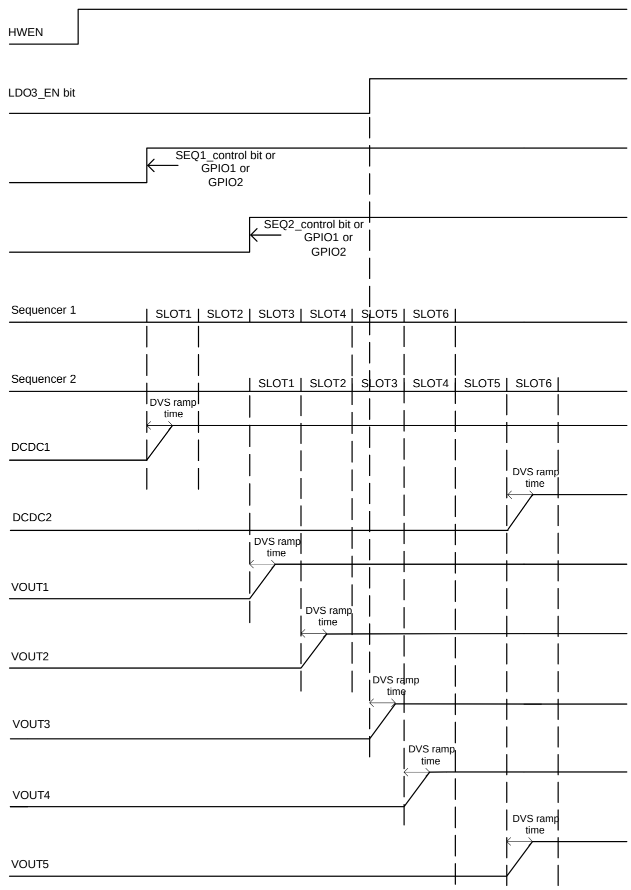


Figure 32.

Example of turn on sequence with DCDC1 assign to SLOT1 SEQ1, DCDC2 assign to SLOT6 SEQ2, VOUT1 assign to SLOT1 SEQ2, VOUT2 assign to SLOT2 SEQ2, VOUT3 control with LDO3_EN bit, VOUT4 assign to SLOT6 SEQ1, VOUT5 assign to SLOT6 SEQ2

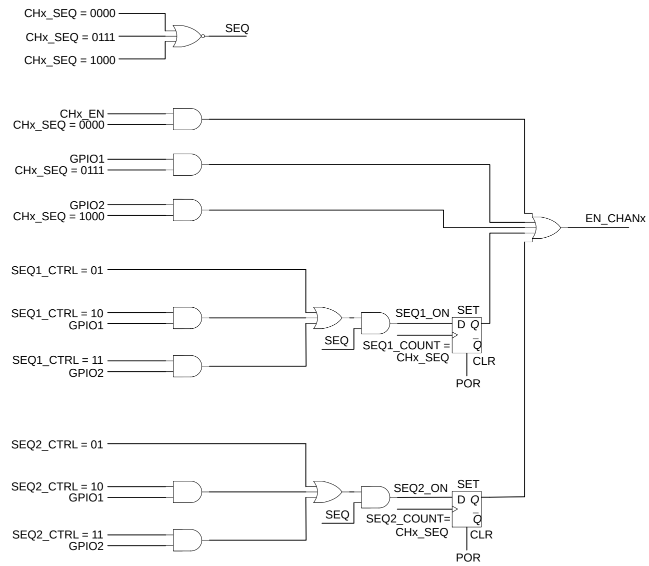


Figure 33. Logic Diagram of Power Up / Power Down

DCDC Step Down Converter and LDO’s Under Voltage Threshold

To indicate that the output of an output channel is established and that the level does not go below 0.875 x Vout_set, a UVT bit is available for each output channel.

The UVT bit is high when the channel is off and goes low when enabling the channel. Once the output voltage reaches the expected output level, the UVT bit becomes high again.

When during operation the output gets below the expected level (87.5% for the LDOs or 90% for the DCDCs) the UVT bit goes low which indicates a power failure. When the voltage rises again above 87.5% for the LDOs or 90% for the DCDCs the UVT bit goes high again.

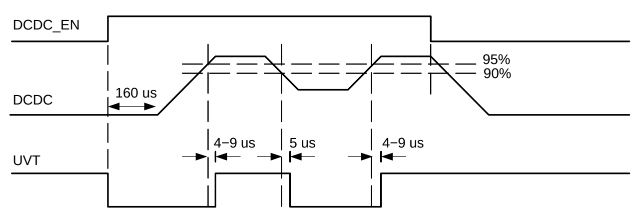


Figure 34. DCDCx Channel Internal UVT Bit

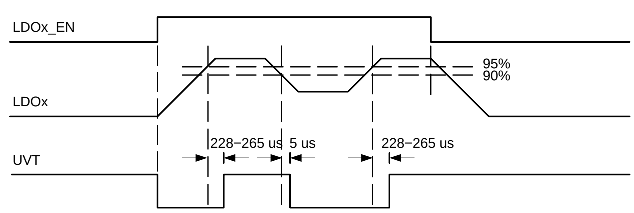


Figure 35. LDOx Channel Internal UVT Bit

Interrupt

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring). The interrupt sources include:

Table 5. INTERRUPT SOURCES

Interrupt Sources	Description
UVT_DCDC1	DCDC1 Under Voltage Threshold
UVT_DCDC2	DCDC2 Under Voltage Threshold
UVT_LDO1	LDO1 Under Voltage Threshold
UVT_LDO2	LDO2 Under Voltage Threshold
UVT_LDO3	LDO3 Under Voltage Threshold
UVT_LDO4	LDO4 Under Voltage Threshold
UVT_LDO5	LDO5 Under Voltage Threshold
UVLO	UVLO state
IDCDC1	DCDC1 Converter Output Over Current
IDCDC2	DCDC2 Converter Output Over Current
ILDO1	LDO1 Output Over Current
ILDO2	LDO2 Output Over Current
ILDO3	LDO3 Output Over Current
ILDO4	LDO4 Output Over Current
ILDO5	LDO5 Output Over Current
ADC_EOC	ADC End Of Conversion
WNRG	Thermal Warning
TSD	Thermal Shutdown

Individual bits generating interrupts will be set to 1 in the INT_ACK1/INT_ACK2/INT_ACK3 registers (I^2C read only registers), indicating the interrupt source. INT_ACK1/INT_ACK2/INT_ACK3 registers are automatically reset by an I^2C read. INT_SEN1/INT_SEN2/INT_SEN3 registers (read only registers) contain real time indicators of interrupt sources.

All interrupt sources can be masked by writing registers INT_MSK1/INT_MSK2/INT_MSK3. Masked sources will never generate an interrupt request on INTB pin.

The INTB pin is an open drain output. A non masked interrupt request will result in the INTB pin being driven low.

When the host reads the INT_ACK1/INT_ACK2/INT_ACK3 registers the INTB pin is released to high impedance and the interrupt registers INT_ACK1/INT_ACK2/INT_ACK3 are cleared.

Below figure shows how DCDC1 converter power good produces interrupt on INTB pin with INT_SEN1/INT_MSK1/INT_ACK1 and an I^2C read access (assuming no other interrupt happens during this read period).

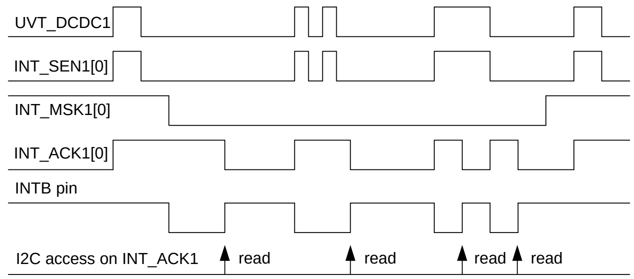


Figure 36. Interrupt Timing Chart Example of PG_DCDC1

INT_MSK1, INT_MSK2 and INT_MSK3 registers are set to disable INTB feature by default during power−up.

In case the interruption is flagged due to an under voltage threshold detection or an output over current detection, the regulator which failed will be turned off.

The regulator can be turn on again only after the INT_ACK1/INT_ACK2/INT_ACK3 registers are cleared by reading these registers.

Errors

The events which are considered as an error and flag the interrupt pin are:

- Under Voltage Threshold of DCDC1
- Under Voltage Threshold of DCDC2
- Under Voltage Threshold of LDO1
- Under Voltage Threshold of LDO2
- Under Voltage Threshold of LDO3
- Under Voltage Threshold of LDO4
- Under Voltage Threshold of LDO5
- Over Current Protection for DCDC1
- Over Current Protection for DCDC2
- Over Current Protection for LDO1
- Over Current Protection for LDO2
- Over Current Protection for LDO3
- Over Current Protection for LDO4
- Over Current Protection for LDO5
- Under Voltage Lock Out
- Thermal Shutdown
- Thermal Shutdown Warning

The errors need to be activated with the registers INT_MASK1/INTMASK2/INT_MASK3.

To recover from the error mode and release the part, the registers INT_ACK1/INT_ACK2/INT_ACK3 has to be read.

- Thermal Shutdown error : When a thermal shutdown event occurs, the part goes in shutdown mode. It recovers in the mode define with the 2 bits REARM[1:0]. By default NCP6925 recovers with a new power up sequence with no reset of the I^2C registers. This error is master and independent of the functionality of the interruption register. The user can choose the flag the INT pin and INT_ACK3 register with the register INT_MSK3.

- Thermal shutdown warning : When a TSD warning event occurs, the INT pin and the INT_ACK3 register are flagged. The user has to read the register INT_ACK3 to recover. This error need to be activated with the registers INT_MASK3. By default this error is masked.
- Under Voltage Lockout : When an under voltage lock out event occurs, the part goes in shutdown mode. It recovers in its default state. This error is master and independent of the functionality of the interruption register. The user can choose to flag the INT pin and INT_ACK1 register with the register INT_MSK1.
- Under Voltage Threshold on CHx: when this event occurs, the corresponding regulator is turned off. The values of CHx_SEQ[3:0] is reset to 0000 and CHx_EN is reset to 0 and the INTB pin is pulled high. This error is linked to the interruption register. By default this error is activated.
- Over Current Protection on CHx: when this event occurs, the corresponding regulator is turned off. The values of CHx_SEQ[3:0] is reset to 0000 and CHx_EN is reset to 0 and the INTB pin is pulled high. This error is linked to the interruption register. By default this error is activated.

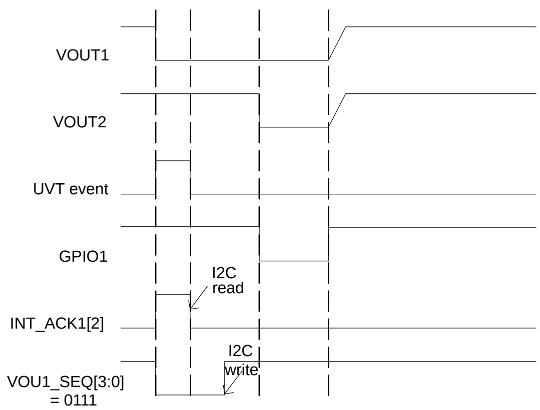


Figure 37. Example for an UVT Event on LDO1 with LDO1 and LDO2 Control by GPIO1

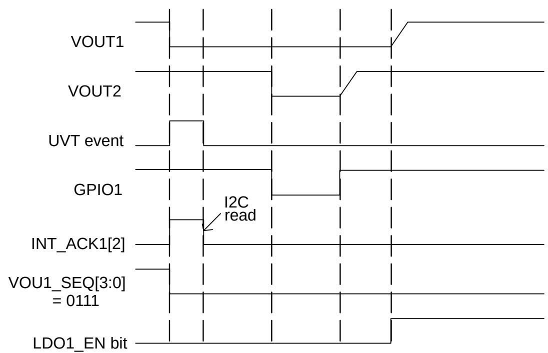


Figure 38. Example for an UVT Event on LDO1 with LDO1 and LDO2 Control by GPIO1 and Restart of the LDO1 with LDO1_EN Bit

GPIOs

2 GPIOs are available and can be configured with GPIO_CONTROL1[] and GPIO_CONTROL2[] register.

GPIO_READ[1:0] bits store the logic level when the pins are set as input.

GPIOx_EN_RD bit set the pin as an input (1) or output (0).

GPIOx[1:0] bits set the logic level (HiZ, low, high) when the pins are set as output.

The GPIOs can also enable or disable one or multiple regulators when it is set as an input and configured in the CHx_SEQ register.

The turn−on or shut down sequence can also be started by a GPIO when it is set as an input and configured in the SEQx_CTRL[1:0] bits.

DCDC Step Down Converters

The DCDC converters are synchronous rectifier type with both high side and low side integrated switches. Neither external transistor nor diodes are required for proper operation. Feedback and compensation network are also fully integrated.

The DCDC converters can operate in two different modes: PWM and PFM. The transition between PWM/PFM modes can occur automatically or the switcher can be placed in forced PWM mode by I^2C programming.

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, DCDC converters operates in PWM mode from a fixed 3MHz clock and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM. The internal N−MOS switch operates as synchronous rectifier and is driven complementary to the P−MOS switch. In CCM the lower (N−MOS switch) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the DCDC converters operate in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N−MOSFET operates as synchronous rectifier after each P−MOSFET on−pulse with very small negative current limit. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM fixed frequency mode.

Forced PWM

The DCDC converters can be programmed to only use PWM and disable the transition to PFM if so desired.

Inductor Peak Current Limitation

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrains inductor power

Soft Start

A soft start is provided to limit inrush currents when enabling the converter. After enabling and internal delays elapsed, the DC to DC converter output will gradually ramp up to the programmed voltage.

Triple Input 10 Bits ADC

The triple input 10 bits has 2 different mode:

During power−up, ADC converts the ADCIN1 and ADCIN2 in the EXTID register.

When HWEN is set, the ADC automatically converts the 2 inputs and then it is turned off. It could be used for applications which need to detect and store in a register the external accessory id when the battery is plugged.

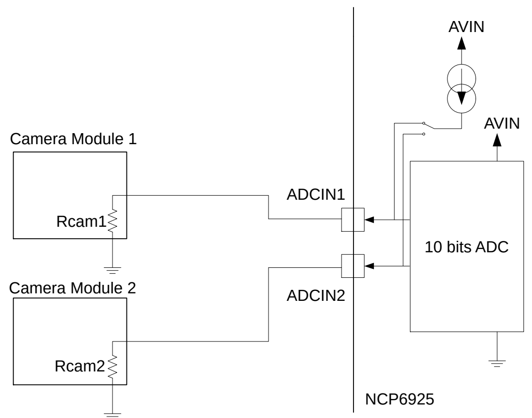


Figure 39. Example for the Detection of 2 External Camera Modules

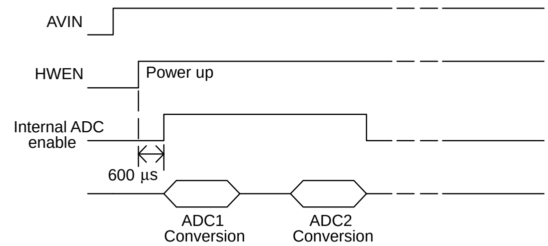


Figure 40. Timing of the 2 Conversion when AVIN is Plugged

When the part is turn on, the 3 inputs of the ADC can be used as a general purpose ADC by setting the ADC_CONF register. Result can be read in the ADC_READ_INPUT register.

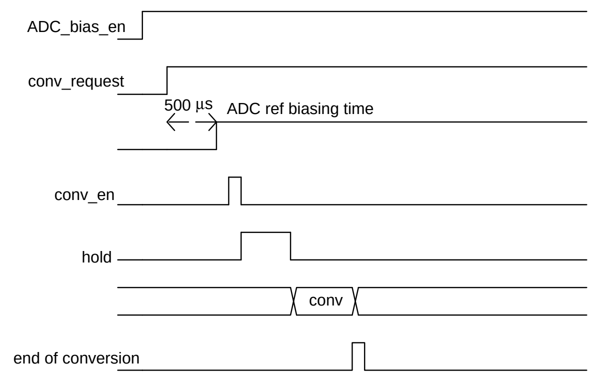


Figure 41. Timing of a Conversion in the General Purpose Mode

I²C COMPATIBLE INTERFACE

NCP6925 can support a subset of I²C protocol, below are detailed introduction for I²C programming.

I²C Communication Description

ON Semiconductor communication protocol is a subset of I²C protocol.

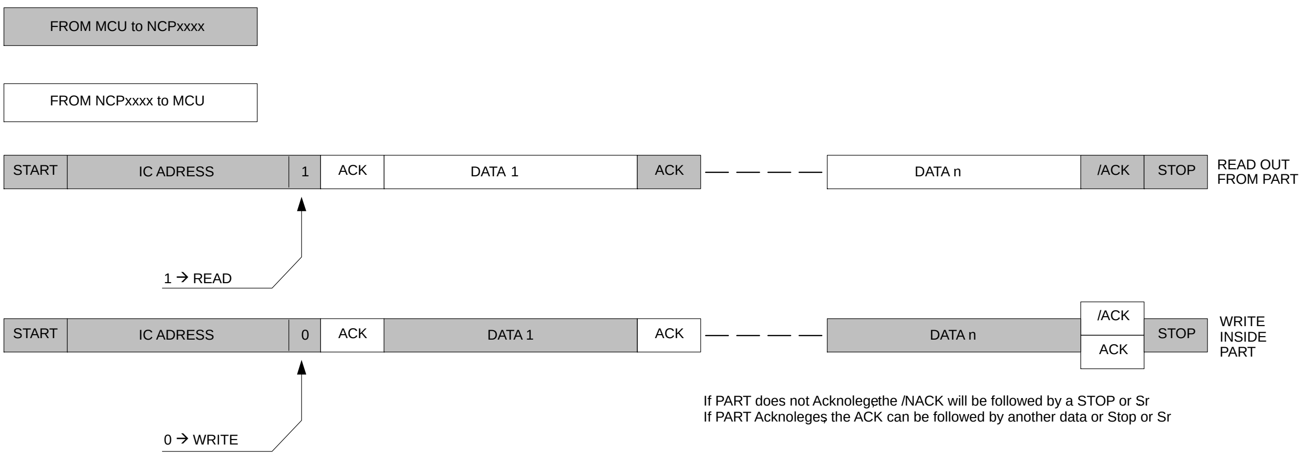


Figure 42. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) we want to write in followed by the data we will write in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1 …. The data are optional.
- In case of read operation, the NCP6925 will output the data out from the last register that has been accessed by the last write operation. Like writing process, reading process is an incremental process.

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set:

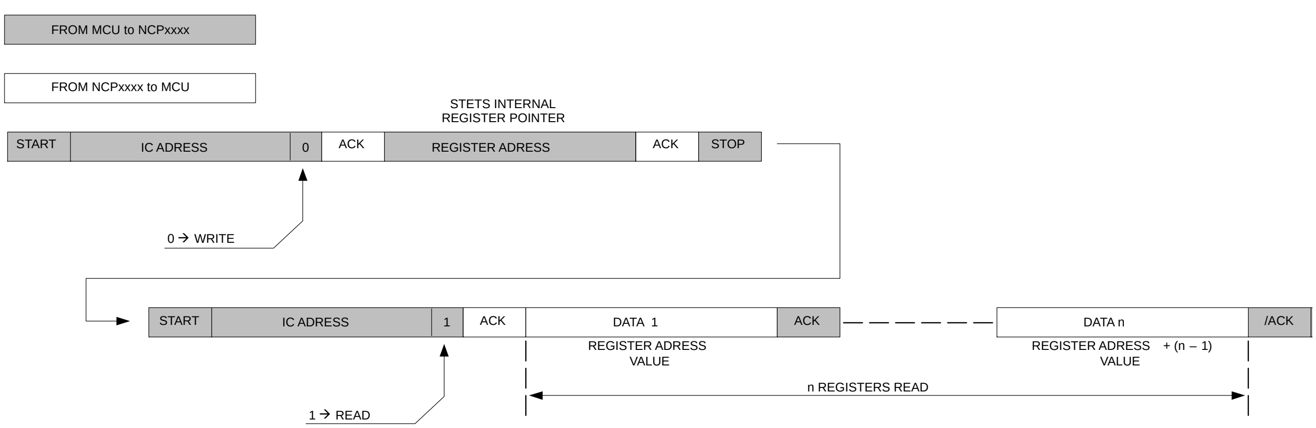


Figure 43. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read:
With Stop Then Start

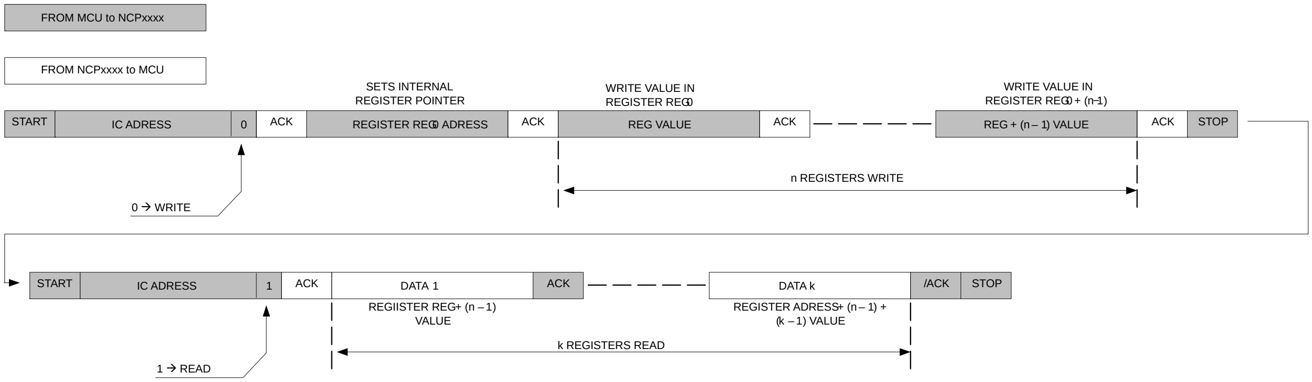


Figure 44. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, …, Reg +n.

Write n Registers:

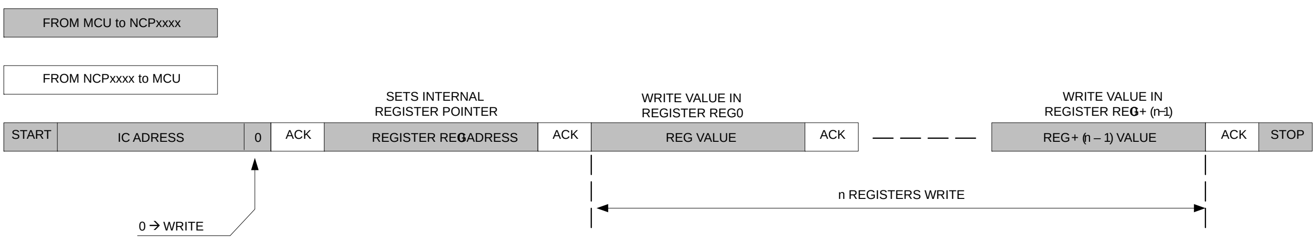


Figure 45. Write in n Registers

I²C Address

NCP6925 has 4 selectable I²C address (see below table A7~A1), NCP6925 supports 7−bit address only.

Table 6. NCP6925 I²C Address

I²C Address		
A1	**A0**	**Hex**
0	0	$50
0	1	$51
1	0	$52
1	1	$53

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
1	0	1	0	0	A1	A0	−

NOTE: Other addresses are available upon request.

Register Map

Following register map describes I²C registers.

Registers can be:

R	Read only register
RC	Read then Clear
RW	Read and Write register
RWM	Read, Write and can be modified by the IC
Reserved	Address is reserved and register is not physically designed
Spare	Address is reserved and register is physically designed

Address	Register Name	Type	Default	Function
$00	CHIP_REV	R	$00	Chip revision
$01	EXT_ID	R	$00	External ID resistor identification
$02	BUCK1_PROG	RW	$00	DCDC1 setting
$03	BUCK2_PROG	RW	$00	DCDC2 setting
$04	BUCKx_PROG	RW	$00	DCDC 1 and 2 setting
$05	LDO1_VOUT	RW	$00	LDO1 output voltage setting
$06	LDO2_VOUT	RW	$00	LDO2 output voltage setting
$07	LDO3_VOUT	RW	$00	LDO3 output voltage setting
$08	LDO4_VOUT	RW	$00	LDO4 output voltage setting
$09	LDO5_VOUT	RW	$00	LDO5 output voltage setting
$0A	–	–	–	–
$0B	CHx_EN	RW	$00	Channel enable register
$0C	BUCKx_SEQ	RW	$00	DCDC 1 and 2 sequencer assignment
$0D	LDO12_SEQ	RW	$00	LDO 1 and 2 sequencer assignment
$0E	LDO34_SEQ	RW	$00	LDO 3 and 4 sequencer assignment
$0F	LDO5_SEQ	RW	$00	LDO 5 sequencer assignment
$10	SEQ1_PROG	RW	$00	Sequencer 1 setting
$11	SEQ2_PROG	RW	$00	Sequencer 2 setting
$12	GPIO_CONTROL1	RW	$00	GPIO 1 and 2 read register
$13	GPIO_CONTROL2	RW	$00	GPIO1 and 2 setting register
$14 to $1F	–	–	–	Reserved for future use
$20	ADC_CONF	RW	$00	ADC configuration register
$21	ADC_READ_INPUT	RW	$00	ADC read input register (bits 2 to 9)
$22	ADC_READ_INPUT2	RW	$00	ADC read input register 2 (bits 0 to 1)
$23	INT_ACK1	RC	$00	Interrupt 1 register (dual edge)
$24	INT_ACK2	RC	$00	Interrupt 2 register (rising edge and dual edge)
$25	INT_ACK3	RC	$00	Interrupt 3 register (rising edge and dual edge)
$26	INT_SEN1	R	$00	Sense 1 register (real time status)
$27	INT_SEN2	R	$00	Sense 2 register (real time status)
$28	INT_SEN3	R	$00	Sense 3 register (real time status)
$29	INT_MASK1	RW	$FF	Mask 1 register to enable or disable interrupt sources
$2A	INT_MASK2	RW	$7F	Mask 2 register to enable or disable interrupt sources
$2B	INT_MASK3	RW	$06	Mask 3 register to enable or disable interrupt sources
$2C	REARM	RW	$01	TSD rearm register setting
$2D	DIS	RW	$7F	Active output discharge register
$2E to $3F	–	–	–	Reserved for future use

0x00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CHIP_REV[7:0]							
Mode	R							
Init	0	0	0	0	0	0	0	0
0x01	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	EXTID2[4:0]				EXTID1[4:0]			

Mode	R				R			
Init	0	0	0	0	0	0	0	0
0x02	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	BUCK1_AUTO	BUCK1_VOUT[6:0]						
Mode	RW	RW						
Init	0	0	0	0	0	0	0	0
0x03	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	BUCK2_AUTO	BUCK2_VOUT[6:0]						
Mode	RW	RW						
Init	0	0	0	0	0	0	0	0
0x04	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name							BUCK2_VOUT[7]	BUCK1_VOUT[7]
Mode							RW	RW
Init							0	0
0x05	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		LDO1_VOUT[6:0]						
Mode		RW						
Init		0	0	0	0	0	0	0
0x06	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		LDO2_VOUT[6:0]						
Mode		RW						
Init		0	0	0	0	0	0	0
0x07	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		LDO3_VOUT[6:0]						
Mode		RW						
Init		0	0	0	0	0	0	0
0x08	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		LDO4_VOUT[6:0]						
Mode		RW						
Init		0	0	0	0	0	0	0
0x09	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		LDO5_VOUT[6:0]						
Mode		RW						
Init		0	0	0	0	0	0	0
0x0A	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name								
Mode								
Init								
0x0B	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		CHx_EN[6:0]						
Mode		RW						
Init		0	0	0	0	0	0	0
0x0C	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	BUCK2_SEQ[3:0]				BUCK1_SEQ[3:0]			

Mode	RW				RW			
Init	0	0	0	0	0	0	0	0
0x0D	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	LDO2_SEQ[3:0]				LDO1_SEQ[3:0]			
Mode	RW				RW			
Init	0	0	0	0	0	0	0	0
0x0E	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	LDO4_SEQ[3:0]				LDO3_SEQ[3:0]			
Mode	RW				RW			
Init	0	0	0	0	0	0	0	0
0x0F	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name					LDO5_SEQ[3:0]			
Mode					RW			
Init					0	0	0	0
0x10	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	SEQ_SPEED[1:0]		SEQ1_CTRL[1:0]		SEQ1_ON	SEQ1_COUNT[2:0]		
Mode	RW		RW		R	R		
Init	0	0	0	0	0	0	0	0
0x11	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name			SEQ2_CTRL[1:0]		SEQ2_ON	SEQ2_COUNT[2:0]		
Mode			RW		R	R		
Init			0	0	0	0	0	0
0x12	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name							GPIO_READ[1:0]	
Mode							R	
Init							0	0
0x13	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		GPIO2[1:0]		GPIO2_EN_RD		GPIO1[1:0]		GPIO1_EN_RD
Mode		RW		RW		RW		RW
Init		0	0	0		0	0	0
0x20	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	ADC_HOLD[2:0]			ADC_CS_DIS	ADC_CHAN[1:0]		ADC_REQ	ADC_EN
Mode	RW			RW	RW		RW	RW
Init	1	1	0	0	0	0	0	0
0x21	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	ADC_READ_INPUT[7:0]							
Mode	R							
Init	0	0	0	0	0	0	0	0
0x22	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name							ADC_READ_INPUT2[1:0]	
Mode							R	
Init							0	0
0x23	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	ACK_UVLO	ACK_UVP_LDO5	ACK_UVP_LDO4	ACK_UVP_LDO3	ACK_UVP_LDO2	ACK_UVP_LDO1	ACK_UVP_DCDC2	ACK_UVP_DCDC1

Mode	RC							
Init	0	0	0	0	0	0	0	0
0x24	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		ACK_ILDO5	ACK_ILDO4	ACK_ILDO3	ACK_ILDO2	ACK_ILDO1	ACK_IDCDC2	ACK_IDCDC1
Mode		RC						
Init		0	0	0	0	0	0	0
0x25	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name						ACK_TSD	ACK_WRNG	ACK_ADCEOC
Mode						RC		
Init						0	0	0
0x26	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	SEN_UVLO	SEN_UVP_LDO5	SEN_UVP_LDO4	SEN_UVP_LDO3	SEN_UVP_LDO2	SEN_UVP_LDO1	SEN_UVP_DCDC2	SEN_UVP_DCDC1
Mode	R							
Init	0	0	0	0	0	0	0	0
0x27	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		SEN_ILDO5	SEN_ILDO4	SEN_ILDO3	SEN_ILDO2	SEN_ILDO1	SEN_IDCDC2	SEN_IDCDC1
Mode		R						
Init		0	0	0	0	0	0	0
0x28	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name							SEN_TSD	SEN_WRNG
Mode							R	
Init							0	0
0x29	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	MSK_UVLO	MSK_UVP_LDO5	MSK_UVP_LDO4	MSK_UVP_LDO3	MSK_UVP_LDO2	MSK_UVP_LDO5	MSK_UVP_DCDC2	MSK_UVP_DCDC1
Mode	RW							
Init	1	1	1	1	1	1	1	1
0x2A	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		MSK_ILDO5	MSK_ILDO4	MSK_ILDO3	MSK_ILDO2	MSK_ILDO1	MSK_IDCDC2	MSK_IDCDC1
Mode		RW						
Init		1	1	1	1	1	1	1
0x2B	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name						MSK_TSD	MSK_WRNG	MSK_ADCEOC
Mode						RW		
Init						1	1	0
0x2C	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name							REARM[1:0]	
Mode							RW	
Init							1	0
0x2D	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name		DIS_LDO5	DIS_LDO4	DIS_LDO3	DIS_LDO3	DIS_LDO1	DIS_DCDC2	DIS_DCDC1
Mode		RW						
Init		1	1	1	1	1	1	1

*Register 0x20 to 0x30 are reserved for internal use only.

REGISTERS DESCRIPTION

Table 7. CHIP_REV REGISTER

Name: CHIP_REV				**Address: $00**			
Type: R				Default: $01			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CHIP_REV[6:0]							

Table 8. BIT DESCRIPTION OF CHIP_REV REGISTER

Bit	Bit Description
CHIP_REV[6:0]	Indicates the device ID with revision

Table 9. EXTID REGISTER

Name: EXTID				**Address: $01**			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
EXTID2[3:0]				EXTID1[3:0]			

Table 10. BIT DESCRIPTION OF EXTID REGISTER

Bit	Bit Description
EXTID1[3:0]	Indicates the ID resistor value placed at ADCIN1
EXTID2[3:0]	Indicates the ID resistor value placed at ADCIN2

Table 11. EXTID REGISTER

ID resistor value (kΩ)	Register value	ID resistor value (kΩ)	Register value
0	0000	220	1000
56	0001	270	1001
68	0010	330	1010
82	0011	390	1011
100	0100	470	1100
120	0101	560	1101
150	0110	680	1110
180	0111	Open (≥ 820)	1111

Table 12. BUCK1_PROG REGISTER

Name: BUCK1_PROG				**Address: $02**			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BUCK1_AUTO	BUCK1_VOUT[6:0]						

Table 13. BUCK2_PROG REGISTER

Name: BUCK1_PROG				**Address: $03**			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BUCK2_AUTO	BUCK2_VOUT[6:0]						

Table 14. BUCK12_PROG REGISTER

Name: BUCK12_PROG				**Address: $04**			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare = 0	spare = 0	spare = 0	spare = 0	spare = 0	spare = 0	BUCK2_VOUT[7]	BUCK1_VOUT[7]

Table 15. BIT DESCRIPTION OF BUCKx_PROG REGISTER

Bit	**Bit Description**
BUCKx_AUTO	0: Fixed PWM operation 1: Auto mode, part enters in PFM mode
BUCKx_VOUT [6:0]	Define the output voltage level of BUCKx.
BUCKx_VOUT[7]	7^{th} bit to define the output voltage level of BUCKx

Table 16. BIT DESCRIPTION OF BUCKx_PROG REGISTER

Bit[7:0]	V_{OUT}(V)	Bit[7:0]	V_{OUT}(V)	Bit[7:0]	V_{OUT}(V)	Bit[7:0]	V_{OUT}(V)	Bit[7:0]	V_{OUT}(V)	Bit[7:0]	V_{OUT}(V)	Bit[7:0]	V_{OUT}(V)
$0	0.6	$20	1	$40	1.4	$60	1.8	$80	2.2	$A0	2.6	$C0	3
$1	0.6125	$21	1.0125	$41	1.4125	$61	1.8125	$81	2.2125	$A1	2.6125	$C1	3.0125
$2	0.625	$22	1.025	$42	1.425	$62	1.825	$82	2.225	$A2	2.625	$C2	3.025
$3	0.6375	$23	1.0375	$43	1.4375	$63	1.8375	$83	2.375	$A3	2.6375	$C3	3.0375
$4	0.65	$24	1.05	$44	1.45	$64	1.85	$84	2.25	$A4	2.65	$C4	3.05
$5	0.6625	$25	1.0625	$45	1.4625	$65	1.8625	$85	2.2625	$A5	2.6625	$C5	3.0625
$6	0.675	$26	1.075	$46	1.475	$66	1.875	$86	2.275	$A6	2.675	$C6	3.075
$7	0.6875	$27	1.0875	$47	1.4875	$67	1.8875	$87	2.2875	$A7	2.6875	$C7	3.0875
$8	0.7	$28	1.1	$48	1.5	$68	1.9	$88	2.3	$A8	2.7	$C8	3.1
$9	0.7125	$29	1.1125	$49	1.5125	$69	1.9125	$89	2.3125	$A9	2.7125	$C9	3.1125
$0A	0.725	$2A	1.125	$4A	1.525	$6A	1.925	$8A	2.325	$AA	2.725	$CA	3.125
$0B	0.7375	$2B	1.1375	$4B	1.5375	$6B	1.9375	$8B	2.3375	$AB	2.7375	$CB	3.1375
$0C	0.75	$2C	1.15	$4C	1.55	$6C	1.95	$8C	2.35	$AC	2.75	$CC	3.15
$0D	0.7625	$2D	1.1625	$4D	1.5625	$6D	1.9625	$8D	2.3625	$AD	2.7625	$CD	3.1625
$0E	0.775	$2E	1.175	$4E	1.575	$6E	1.975	$8E	2.375	$AE	2.775	$CE	3.175
$0F	0.785	$2F	1.1875	$4F	1.5875	$6F	1.9875	$8F	2.3875	$AF	2.7875	$CF	3.1875
$10	0.8	$30	1.2	$50	1.6	$70	2	$90	2.4	$B0	2.8	$D0	3.2
$11	0.8125	$31	1.2125	$51	1.6125	$71	2.0125	$91	2.4125	$B1	2.8125	$D1	3.2125
$12	0.825	$32	1.225	$52	1.625	$72	2.025	$92	2.425	$B2	2.825	$D2	3.225
$13	0.8375	$33	1.2375	$53	1.6375	$73	2.0375	$93	2.4375	$B3	2.8375	$D3	3.2375
$14	0.85	$34	1.25	$54	1.65	$74	2.05	$94	2.45	$B4	2.85	$D4	3.25
$15	0.8625	$35	1.2625	$55	1.6625	$75	2.0625	$95	2.4625	$B5	2.8625	$D5	3.2625
$16	0.875	$36	1.275	$56	1.675	$76	2.075	$96	2.475	$B6	2.875	$D6	3.275
$17	0.8875	$37	1.2875	$57	1.6875	$77	2.0875	$97	2.4875	$B7	2.8875	$D7	3.2875
$18	0.9	$38	1.3	$58	1.7	$78	2.1	$98	2.5	$B8	2.9	$D8	3.3
$19	0.9125	$39	1.3125	$59	1.7125	$79	2.1125	$99	2.5125	$B9	2.9125		
$1A	0.925	$3A	1.325	$5A	1.725	$7A	2.125	$9A	2.525	$BA	2.925		
$1B	0.9375	$3B	1.3375	$5B	1.7375	$7B	2.1375	$9B	2.5375	$BB	2.9375		
$1C	0.95	$3C	1.35	$5C	1.75	$7C	2.15	$9C	2.55	$BC	2.95		
$1D	0.9625	$3D	1.3625	$5D	1.7625	$7D	2.1625	$9D	2.5625	$BD	2.9625		
$1E	0.975	$3E	1.375	$5E	1.775	$7E	2.175	$9E	2.575	$BE	2.975		
$1F	0.9875	$3F	1.3875	$5F	1.7875	$7F	2.1875	$9F	2.5875	$BF	2.9875		

Table 17. LDO1_VOUT REGISTER

Name: LDO1_VOUT				Address: $05			
Type: RW				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	LDO1_VOUT[6:0]						

Table 18. LDO2_VOUT REGISTER

Name: LDO2_VOUT				Address: $06			
Type: RW				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	LDO2_VOUT[6:0]						

Table 19. LDO3_VOUT REGISTER

Name: LDO3_VOUT				Address: $07			
Type: RW				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	LDO3_VOUT[6:0]						

Table 20. LDO4_VOUT REGISTER

Name: LDO4_VOUT				Address: $08			
Type: RW				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	LDO4_VOUT[6:0]						

Table 21. LDO5_VOUT REGISTER

Name: LDO5_VOUT				Address: $09			
Type: RW				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	LDO5_VOUT[6:0]						

Table 22. BIT DESCRIPTION OF LDOx_VOUT REGISTER

Bit[6:0]	V_{OUT}(V)	Bit [6:0]	V_{OUT}(V)	Bit [6:0]	V_{OUT}(V)	Bit [6:0]	V_{OUT}(V)
$00	0.8	$23	1.375	$46	2.25	$69	3.125
$01	0.8	$24	1.4	$47	2.275	$6A	3.15
$02	0.8	$25	1.425	$48	2.3	$6B	3.175
$03	0.8	$26	1.45	$49	2.325	$6C	3.2
$04	0.8	$27	1.475	$4A	2.35	$6D	3.225
$05	0.8	$28	1.5	$4B	2.375	$6E	3.25
$06	0.8	$29	1.525	$4C	2.4	$6F	3.275
$07	0.8	$2A	1.55	$4D	2.425	$70	3.3
$08	0.8	$2B	1.575	$4E	2.45	$71	3.325
$09	0.8	$2C	1.6	$4F	2.475	$72	3.35
$0A	0.8	$2D	1.625	$50	2.5	$73	3.375
$0B	0.8	$2E	1.65	$51	2.525	$74	3.4
$0C	0.8	$2F	1.675	$52	2.55	$75	3.425
$0D	0.825	$30	1.7	$53	2.575	$76	3.45

Table 22. BIT DESCRIPTION OF LDOx_VOUT REGISTER

Bit[6:0]	V_{OUT}(V)	Bit [6:0]	V_{OUT}(V)	Bit [6:0]	V_{OUT}(V)	Bit [6:0]	V_{OUT}(V)
$0E	0.85	$31	1.725	$54	2.6	$77	3.475
$0F	0.875	$32	1.75	$55	2.625	$78	3.5
$10	0.9	$33	1.775	$56	2.65	$79	3.5
$11	0.925	$34	1.8	$57	2.675	$7A	3.5
$12	0.95	$35	1.825	$58	2.7	$7B	3.5
$13	0.975	$36	1.85	$59	2.725	$7C	3.5
$14	1	$37	1.875	$5A	2.75	$7D	3.5
$15	1.025	$38	1.9	$5B	2.775	$7E	3.5
$16	1.05	$39	1.925	$5C	2.8	$7F	Full ON
$17	1.075	$3A	1.95	$5D	2.825		
$18	1.1	$3B	1.975	$5E	2.85		
$19	1.125	$3C	2	$5F	2.875		
$1A	1.15	$3D	2.025	$60	2.9		
$1B	1.175	$3E	2.05	$61	2.925		
$1C	1.2	$3F	2.075	$62	2.95		
$1D	1.225	$40	2.1	$63	2.975		
$1E	1.25	$41	2.125	$64	3		
$1F	1.275	$42	2.15	$65	3.025		
$20	1.3	$43	2.175	$66	3.05		
$21	1.325	$44	2.2	$67	3.075		
$22	1.35	$45	2.225	$68	3.1		

Table 23. CHx_EN REGISTER

Name: CHx_EN				Address: $0B			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	CHx_EN[6:0]						

Table 24. BIT DESCRIPTION OF CHx_EN REGISTER

Bit	Bit Description
CHx_EN[6:0]	Enable bit of each regulator In case the regulators are set to be controlled by I^2C (BUCKx / LDOx_SEQ[1:0], this register can be written to enable or disable the corresponding regulator. In case the regulators are set to follow SEQx or GPIOx, this register should be read only

Table 25. BIT DESCRIPTION OF CHx_EN REGISTER

Register Value	VOUTx	Register Value	VOUTx
Bit 0	BUCK 1	Bit 4	LDO 3
Bit 1	BUCK 2	Bit 5	LDO 4
Bit 2	LDO 1	Bit 6	LDO 5
Bit 3	LDO2		

Table 26. BUCKx_SEQ REGISTER

Name: BUCKx_SEQ				Address: $0C			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BUCK2_SEQ[3:0]				BUCK1_SEQ[3:0]			

Table 27. LDO12_SEQ REGISTER

Name: LDO12_SEQ				Address: $0D			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO2_SEQ[3:0]				LDO1_SEQ[3:0]			

Table 28. LDO34_SEQ REGISTER

Name: LDO34_SEQ				Address: $0E			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO4_SEQ[3:0]				LDO3_SEQ[3:0]			

Table 29. LDO5_SEQ REGISTER

Name: LDO5_SEQ				Address: $0F			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	spare=0	spare=0	LDO5_SEQ[3:0]			

Table 30. BIT DESCRIPTION OF CHx_SEQ REGISTER

Bit	Bit Description
CHx_SEQ[3:0]	This register defines how to power−up and shutdown the corresponding regulator. 2 sequence group are available (SEQ1 and SEQ2), and each group has 6 time slots. Power−up and shutdown of each regulator can be set at one slot of one sequence, or by GPIO control or by I^2C with CHx_CTRL

Table 31. BIT DESCRIPTION OF CHx_SEQ REGISTER

Register Value	VOUTx Sequence	Register Value	VOUTx Sequence
0000	Controlled by I^2C with CH_x_EN[x]	1000	Controlled by GPIO2
0001	SLOT1 of SEQ1	1001	SLOT1 of SEQ2
0010	SLOT2 of SEQ1	1010	SLOT2 of SEQ2
0011	SLOT3 of SEQ1	1011	SLOT3 of SEQ2
0100	SLOT4 of SEQ1	1100	SLOT4 of SEQ2
0101	SLOT5 of SEQ1	1101	SLOT5 of SEQ2
0110	SLOT6 of SEQ1	1110	SLOT6 of SEQ2
0111	Controlled by GPIO1	1111	Not Applicable

Table 32. SEQ1_PROG REGISTER

Name: SEQ1_PROG				Address: $10			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEQ_SPEED[1:0]		SEQ1_CTRL[1:0]		SEQ1_ON	SEQ1_COUNT[2:0]		

Table 33. SEQ2_PROG REGISTER

Name: SEQ2_PROG				Address: $11			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	SEQ2_CTRL[1:0]		SEQ2_ON	SEQ2_COUNT[2:0]		

Table 34. BIT DESCRIPTION OF SEQx_PROG REGISTER

Bit	Bit Description
SEQ_SPEED[1:0]	Defines the SLOT period for SEQx and softstart time
SEQx_CTRL[1:0]	Enables power−up or shutdown of SEQx or assign GPIOx to control SEQx.
SEQx_COUNT[2:0]	Indicates the SLOT number of SEQx at the moment
SEQx_ON	This bit is read only. It indicates the status of the internal SEQx_ON signal

Table 35. BIT DESCRIPTION OF SEQ_SPEED REGISTER

Register Value	SLOT period (ms)	DCDC Softstart time (ms)
00	2.73	$0.853_{(ms/V)}$ x Vout
01	1.365	$0.427_{(ms/V)}$ x Vout
10	0.682	$0.213_{(ms/V)}$ x Vout
11	0.341	$0.107_{(ms/V)}$ x Vout

Table 36.
BIT DESCRIPTION OF SEQx_CTRL REGISTER

Register Value	SEQx_control
00	Shutdown
01	Power−up
10	Assign GPIO1 to control SEQx
11	Assign GPIO2 to control SEQx

Table 37.
BIT DESCRIPTION OF SEQx_COUNT REGISTER

Register Value	SEQx_count
000	No SEQx has been started
001	SLOT1
010	SLOT2
011	SLOT3
100	SLOT4
101	SLOT5
110	SLOT6
111	SEQx completed

Table 38. GPIO_CONTROL1 REGISTER

Name: GPIO_CONTROL1				Address: $12			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare=0	Spare=0	Spare=0	Spare=0	Spare=0	Spare=0	GPIO_READ[1:0]	

Table 39. GPIO_CONTROL2 REGISTER

Name: GPIO_CONTROL1				Address: $13			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare=0	GPIO2[1:0]		GPIO2_EN_RD	Spare=0	GPIO1[1:0]		GPIO1_EN_RD

Table 40. BIT DESCRIPTION OF SEQx_PROG REGISTER

Bit	Bit Description
GPIO_READ[1:0]	Logic input state of GPIOx. In case GPIO_EN_RD = 0, the corresponding GPIO_READ[] is 0
GPIOx_EN_RD	Enable input buffer of GPIOx
GPIOx[1:0]	Output control of GPIOx

Table 41.
BIT DESCRIPTION OF GPIO_READ REGISTER

Register Value	Function
Bit 0	GPIO1 logic input
Bit 1	GPIO2 logic input

Table 42.
BIT DESCRIPTION OF GPIOx_EN_RD REGISTER

Register Value	Function
0	Disable input buffer
1	Enable input buffer. Input logic state will be stored at GPIO_READ[]

Table 43. BIT DESCRIPTION OF GPIOx[1:0] REGISTER

Register Value	Function
00	Hi−Z
01	Hi−Z
10	Logic Low
11	Logic High

Table 44. ADC_CONF REGISTER

Name: ADC_CONFIG				Address: $20			
Type: RW				Default: $C0			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADC_HOLD[2:0]			ADC_CS_DIS	ADC_CHAN[1:0]		ADC_REQ	ADC_BIAS_EN

Table 45. BIT DESCRIPTION OF ADC_CONF REGISTER

Bit	Bit Description
ADC_BIAS_EN	Enable bit for the 10 bits ADC.
ADC_REQ	ADC start conversion, self cleared when conversion done
ADC_CHAN[1:0]	ADC channel selection
ADC_CS_DIS	ADC input current source disable bit. Write 1 to disable. (available only for input 1 and 2)
ADC_HOLD	Defines the hold time for the conversion

Table 46.
BIT DESCRIPTION OF ADC_CHAN[1:0] REGISTER

Register Value	Function
00	Channel 1
01	Channel 2
10	Channel 3
11	Channel 3

Table 47.
BIT DESCRIPTION OF ADC_HOLD[2:0] REGISTER

Register Value	Clock Periods
000	Reserved
001	Reserved
010	Reserved
011	Reserved
100	64
101	96
110	128
111	256

Table 48. ADC_READ_INPUT REGISTER

Name: ADC_READ_INPUT				Address: $21			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADC_READ_INPUT[7:0]							

Table 49. BIT DESCRIPTION OF ADC_READ_INPUT REGISTER

Bit	Bit Description
ADC_READ_INPUT[7:0]	This register returns the bits 2 to 9 of ADC.

Table 50. ADC_READ_INPUT2 REGISTER

Name: ADC_READ_INPUT 2				Address: $22			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
						ADC_READ_INPUT2[1:0]	

Table 51. BIT DESCRIPTION OF ADC_READ_INPUT REGISTER

Bit	Bit Description
ADC_READ_INPUT2[1:0]	This register returns the bits 0 and 1 of ADC.

Table 52. INT_ACK1 REGISTER

Name: INT_ACK1				Address: $23			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ACK_UVLO	ACK_UVT_LDO5	ACK_UVT_LDO4	ACK_UVT_LDO3	ACK_UVT_LDO2	ACK_UVT_LDO1	ACK_UVT_DCDC2	ACK_UVT_DCDC1

Table 53. BIT DESCRIPTION OF INT_ACK1 REGISTER

Bit	Bit Description
ACK_UVT_DCDC1	DCDC1 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: DCDC1 Under Voltage Threshold Event detected
ACK_UVT_DCDC2	DCDC2 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: DCDC2 Under Voltage Threshold Event detected
ACK_UVT_LDO1	LDO1 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: LDO1 Under Voltage Threshold Event detected
ACK_UVT_LDO2	LDO2 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: LDO2 Under Voltage Threshold Event detected
ACK_UVT_LDO3	LDO3 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: LDO3 Under Voltage Threshold Event detected
ACK_UVT_LDO4	LDO4 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: LDO4 Under Voltage Threshold Event detected
ACK_UVT_LDO5	LDO5 Under Voltage Threshold Sense Acknowledgement 0: Cleared 1: LDO5 Under Voltage Threshold Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected

Table 54. INT_ACK2 REGISTER

Name: INT_ACK2				Address: $24			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	ACK_ILDO5	ACK_ILDO4	ACK_ILDO3	ACK_ILDO2	ACK_ILDO1	ACK_IDCDC2	ACK_IDCDC 1

Table 55. BIT DESCRIPTION OF INT_ACK2 REGISTER

Bit	Bit Description
ACK_IDCDC1	DCDC1 Over Current Sense Acknowledgement 0: Cleared 1: DCDC1 Over Current Event detected
ACK_IDCDC2	DCDC2 Over Current Sense Acknowledgement 0: Cleared 1: DCDC2 Over Current Event detected
ACK_ILDO1	LDO1 Over Current Sense Acknowledgement 0: Cleared 1: LDO1 Over Current Event detected
ACK_ILDO2	LDO2 Over Current Sense Acknowledgement 0: Cleared 1: LDO2 Over Current Event detected
ACK_ILDO3	LDO3 Over Current Sense Acknowledgement 0: Cleared 1: LDO3 Over Current Event detected
ACK_ILDO4	LDO4 Over Current Sense Acknowledgement 0: Cleared 1: LDO4 Over Current Event detected
ACK_ILDO5	LDO5 Over Current Sense Acknowledgement 0: Cleared 1: LDO5 Over Current Event detected

Table 56. INT_ACK3 REGISTER

Name: INT_ACK3				Address: $25			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	spare=0	spare=0	spare=0	ACK_TSD	ACK_WNRG	ACK_ADCEOC

Table 57. BIT DESCRIPTION OF INT_ACK3 REGISTER

Bit	Bit Description
ACK_ADCEOC	ADC End Of Conversion Acknowledgement 0: Cleared 1: ADC End Of Conversion detected
ACK_WNRG	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 58. INT_SEN1 REGISTER

Name: INT_SEN1				Address: $26			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_UVLO	SEN_UVT_LDO5	SEN_UVT_LDO4	SEN_UVT_LDO3	SEN_UVT_LDO2	SEN_UVT_LDO1	SEN_UVT_DCDC2	SEN_UVT_DCDC1

Table 59. BIT DESCRIPTION OF INT_SEN1 REGISTER

Bit	Bit Description
SEN_UVT_DCDC1	DCDC1 Under Voltage Threshold Sense 0: DCDC1 Output Voltage below target 1: DCDC1 Output Voltage within nominal range
SEN_UVT_DCDC2	DCDC2 Under Voltage Threshold Sense 0: DCDC2 Output Voltage below target 1: DCDC2 Output Voltage within nominal range
SEN_UVT_LDO1	LDO1 Under Voltage Threshold Sense 0: LDO1 Output Voltage below target 1: LDO1 Output Voltage within nominal range
SEN_UVT_LDO2	LDO2 Under Voltage Threshold Sense 0: LDO2 Output Voltage below target 1: LDO2 Output Voltage within nominal range
SEN_UVT_LDO3	LDO3 Under Voltage Threshold Sense 0: LDO3 Output Voltage below target 1: LDO3 Output Voltage within nominal range
SEN_UVT_LDO4	LDO4 Under Voltage Threshold Sense 0: LDO4 Output Voltage below target 1: LDO4 Output Voltage within nominal range
SEN_UVT_LDO5	LDO5 Under Voltage Threshold Sense 0: LDO5 Output Voltage below target 1: LDO5 Output Voltage within nominal range
SEN_UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold

Table 60. INT_SEN2 REGISTER

Name: INT_SEN2				Address: $27			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	SEN_ILDO5	SEN_ILDO4	SEN_ILDO3	SEN_ILDO2	SEN_ILDO1	SEN_IDCDC2	SEN_IDCDC1

Table 61. BIT DESCRIPTION OF INT_SEN2 REGISTER

Bit	Bit Description
SEN_IDCDC1	DCDC1 Over Current Sense 0: DCDC1 Output Current below limit 1: DCDC1 Output Current over limit
SEN_IDCDC2	DCDC2 Over Current Sense 0: DCDC2 Output Current below limit 1: DCDC2 Output Current over limit
SEN_ILDO1	LDO1 Over Current Sense 0: LDO1 Output Current below limit 1: LDO1 Output Current over limit
SEN_ILDO2	LDO2 Over Current Sense 0: LDO2 Output Current below limit 1: LDO2 Output Current over limit
SEN_ILDO3	LDO3 Over Current Sense 0: LDO3 Output Current below limit 1: LDO3 Output Current over limit
SEN_ILDO4	LDO4 Over Current Sense 0: LDO4 Output Current below limit 1: LDO4 Output Current over limit
SEN_ILDO5	LDO5 Over Current Sense 0: LDO5 Output Current below limit 1: LDO5 Output Current over limit

Table 62. INT_SEN3 REGISTER

Name: INT_SEN3				Address: $28			
Type: R				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	spare=0	spare=0	spare=0	spare=0	SEN_TSD	SEN_WNRG

Table 63. BIT DESCRIPTION OF INT_SEN3 REGISTER

Bit	Bit Description
SEN_WNRG	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN_TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 64. INT_MSK1 REGISTER

Name: INT_MSK1				Address: $29			
Type: RW				Default: $FF			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MSK_UVLO	MSK_UVT_LDO5	MSK_UVT_LDO4	MSK_UVT_LDO3	MSK_UVT_LDO2	MSK_UVT_LDO1	MSK_UVT_DCDC2	MSK_UVT_DCDC1

Table 65. BIT DESCRIPTION OF INT_MSK1 REGISTER

Bit	Bit Description
MSK_UVT_DCDC1	DCDC1 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVT_DCDC2	DCDC2 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVT_LDO1	LDO1 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVT_LDO2	LDO2 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVT_LDO3	LDO3 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVT_LDO4	LDO4 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVT_LDO5	LDO5 Under Voltage Threshold Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVLO	UVLO Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 66. INT_MSK2 REGISTER

Name: INT_MSK2				Address: $2A			
Type: RW				Default: $7F			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	MSK_ILDO5	MSK_ILDO4	MSK_ILDO3	MSK_ILDO2	MSK_ILDO1	MSK_IDCDC2	MSK_IDCDC1

Table 67. BIT DESCRIPTION OF INT_MSK2 REGISTER

Bit	Bit Description
MSK_IDCDC1	DCDC1 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_IDCDC2	DCDC2 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO1	LDO1 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO2	LDO2 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO3	LDO3 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO4	LDO4 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO5	LDO5 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 68. INT_MSK3 REGISTER

Name: INT_MSK3				Address: $2B			
Type: RW				Default: $06			
D7	D6	D5	D4	D3	D2	D1	D0
spare=0	spare=0	spare=0	spare=0	spare=0	MSK_TSD	MSK_WNRG	MSK_ADCEOC

Table 69. BIT DESCRIPTION OF INT_MSK3 REGISTER

Bit	Bit Description
MSK_ADCEOC	ADC End Of Charge Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_WNRG	Thermal Warning Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TSD	Thermal Shutdown Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 70. REARM REGISTER

Name: REARM				Address: $2C			
Type: RW				Default: $01			
D7	D6	D5	D4	D3	D2	D1	D0
spare=0	spare=0	spare=0	spare=0	spare=0	spare=0	REARM[1:0]	

Table 71. BIT DESCRIPTION OF REARM REGISTER

Bit	Bit Description
REARM[1:0]	Rearming of device after TSD

Table 72. BIT DESCRIPTION OF REARM[1:0] REGISTER

Register Value	Function
00	Re−arming active after TSD with reset of I^2C registers : new power−up sequence is initiated with default I^2C register values
01	Re−arming active after TSD with no reset of I^2C registers : new power−up sequence is initiated with I^2C registers values
10	No re−arming after TSD
11	NA

Table 73. DIS REGISTER

Name: DIS				Address: $2D			
Type: RW				Default: $7F			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	DIS_DCDC2	DIS_DCDC1	DIS_LDO5	DIS_LDO4	DIS_LDO3	DIS_LDO2	DIS_LDO1

Table 74. BIT DESCRIPTION OF DIS REGISTER

Bit	Bit Description
DIS_LDO1	LDO1 active output discharge 0: Disabled 1: Enabled
DIS_LDO2	LDO2 active output discharge 0: Disabled 1: Enabled
DIS_LDO3	LDO3 active output discharge 0: Disabled 1: Enabled
DIS_LDO4	LDO4 active output discharge 0: Disabled 1: Enabled
DIS_LDO5	LDO5 active output discharge 0: Disabled 1: Enabled
DIS_DCDC1	DCDC1 active output discharge 0: Disabled 1: Enabled
DIS_DCDC2	DCDC2 active output discharge 0: Disabled 1: Enabled

Application Information

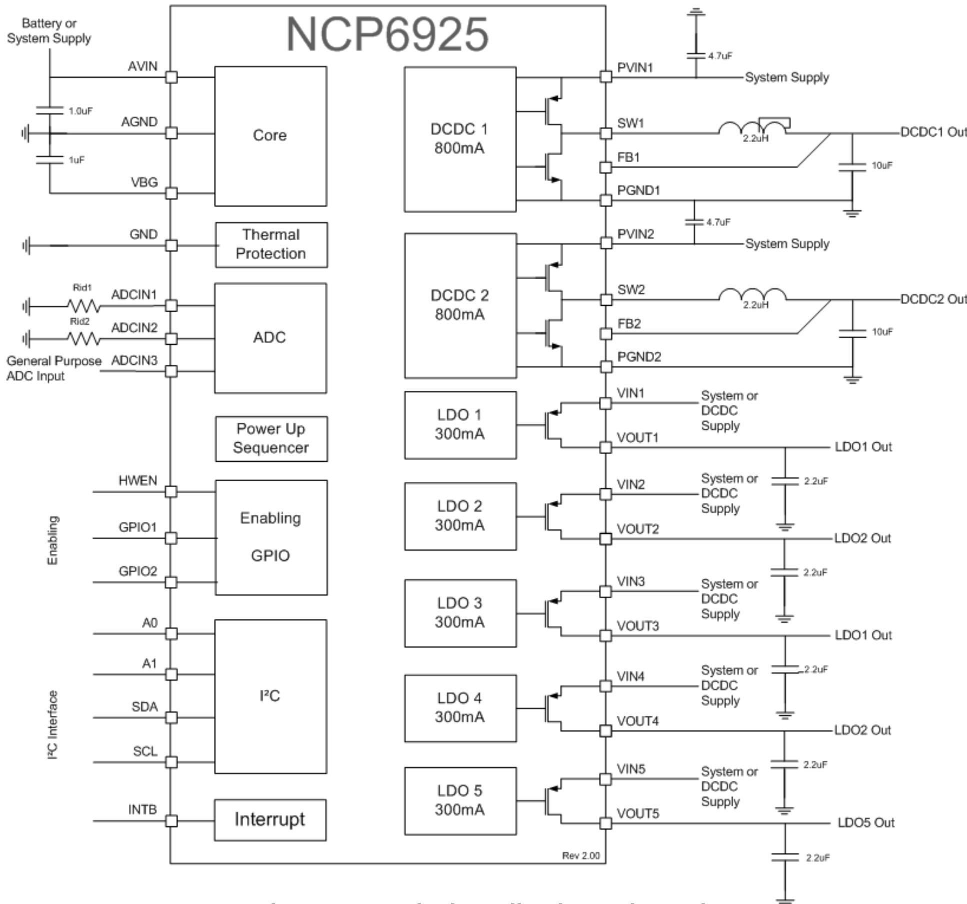


Figure 46. Typical Application Schematic

Inductor Selection

NCP6925 DCDC converters typically use 1 μH inductor. Use of different values can be considered to optimize operation in specific conditions. The inductor parameters directly related to device performances are saturation current, DC resistance and inductance value. The inductor ripple current (ΔIL) decreases with higher inductance.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \qquad \text{(eq. 1)}$$

$$I_{LMAX} = I_{OMAX} + \frac{\Delta I_L}{2} \qquad \text{(eq. 2)}$$

With:

- Fsw = Switching Frequency (Typical 3 MHz)
- L = Inductor value
- ΔI_L = Peak−To−Peak inductor ripple current
- I_{LMAX} = Maximum Inductor Current

To achieve better efficiency, ultra low DC resistance inductor should be selected.

The saturation current of the inductor should be higher than the I_{LMAX} calculated with the above equations.

Table 75. INDUCTOR L = 1.0 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
MURATA	LQH44PN−1R0NP0	4.0 x 3.5 x 1.8	2.5	36
MURATA	LQM2HPN−1R0MG0	2.5 x 2.0 x 1.0	1.6	69
TOKO	DFE252012C−1R0N	2.5 x 2.0 x 1.2	3.0	59
TOKO	DFE252012R−1R0N	2.5 x 2.0 x 1.2	3.4	49
TOKO	DFE201612R−1R0N	2.0 x 1.6 x 1.2	2.6	70

Table 76. INDUCTOR L = 2.2 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
MURATA	LQH44PN−2R2MP0	4.0 x 3.5 x 1.8	1.8	59
MURATA	LQM2HPN−2R2MG0	2.5 x 2.0 x 1.0	1.3	100
TOKO	DFE252012C−2R2N	2.5 x 2.0 x 1.2	2.0	108
TOKO	DFE252012R−2R2N	2.5 x 2.0 x 1.2	2.4	90
TOKO	DFE201612R−2R2N	2.0 x 1.6 x 1.2	1.7	154

Output Capacitor Selection for DC to DC Converters

Selecting the proper output capacitor is based on the desired output ripple voltage. NCP6925 DCDC converters typically use 10 μF output capacitor. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode can be estimated by:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \times \left(\frac{1}{2 \times \pi \times C_O \times f} + ESR \right) \quad \text{(eq. 3)}$$

Table 77. RECOMMENDED OUTPUT CAPACITOR FOR DC TO DC CONVERTERS

Manufacturer	Part Number	Case Size	HeightTyp. [mm]	C [uF]
MURATA	GRM188R60J106ME47	0603	0.8	10
MURATA	GRM219R60J106KE19	0805	1.25	10
MURATA	GRM21BR60J226ME39	0805	1.25	22
TDK	C1608X5R0C106K/M	0603	0.8	10
TDK	C2012X5R0C106K/M	0805	1.25	10
TDK	C2012X5R0C226K/M	0805	1.25	22

Input Capacitor Selection for DC TO DC Converters

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is 1/2 of maximum output current. A low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to PVIN1 and PVIN2 pins.

Table 78. RECOMMENDED INPUT CAPACITOR FOR DC TO DC CONVERTERS

Supplier	Part Number	CaseSize	Height Typ. [mm]	C [uF]
MURATA	GRM188R60J475KE	0603	0.8	4.7
MURATA	GRM188R60J106ME	0603	0.8	10
TDK	C1608X5R0C475K/M	0603	0.8	4.7
TDK	C1608X5R0C106K/M	0603	0.8	10

Output Capacitor for LDOs

For stability reason, a typical 2.2 μF ceramic output capacitor is suitable for LDOs. The LDO output capacitor should be placed as close as possible to the NCP6925 output pin.

Input Capacitor for LDOs

NCP6925 LDOs do not require specific input capacitors. However, a typical 1 μF ceramic capacitor placed close to LDOs' input is helpful for load transient.

Power input of LDO can be connected to main power supply. However, for optimum efficiency and lower NCP6925 thermal dissipation, the lowest voltage available in the system is preferred. Input voltage of each LDO should always be higher than V_{OUT} + $V_{LDODROP}$ (V_{DROP}, LDO dropout voltage at maximum current).

Capacitor DC Bias Characteristics

Real capacitance of ceramic capacitor changes versus DC voltage. Special care should be taken to DC bias effect in order to make sure that the real capacitor value is always higher than the minimum allowable capacitor value specified.

PCB Layout Recommendation

The high speed operation of the NCP6925 demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.

Both the inductor and input/output capacitor of each DC to DC converters are in the high frequency switching path where current flow may be discontinuous. These components should be placed as close to NCP6925 as possible to reduce parasitic inductance connection. Also it is important to minimize the area of the switching nodes and use the ground plane under them to minimize cross−talk to sensitive signals and ICs. It's suggested to keep as complete of a ground plane under NCP6925 as possible.

PGND and AGND pin connection must be connected to the ground plane. Care should be taken to avoid noise interference between PGND and AGND.

It is always good practice to keep the sensitive tracks such as feedback connection (FB1 / FB2) away from switching signal connections (SW1 / SW2) by laying the tracks on the other side or inner layers of PCB.

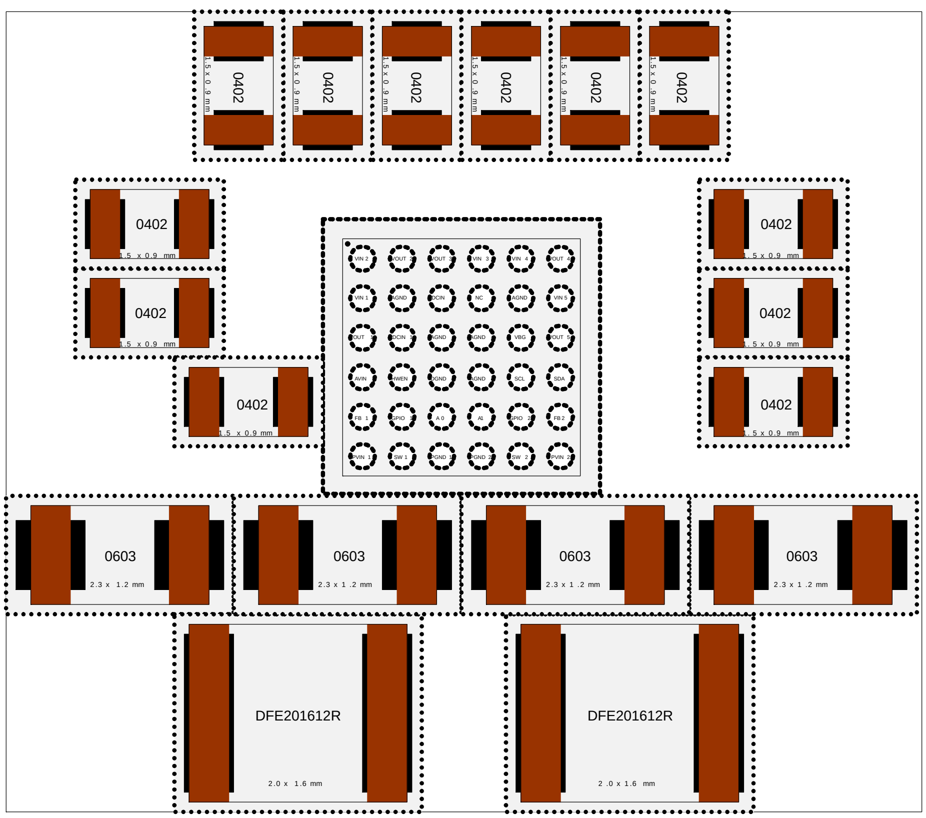


Figure 47. Recommended PCB Assembly (top view)

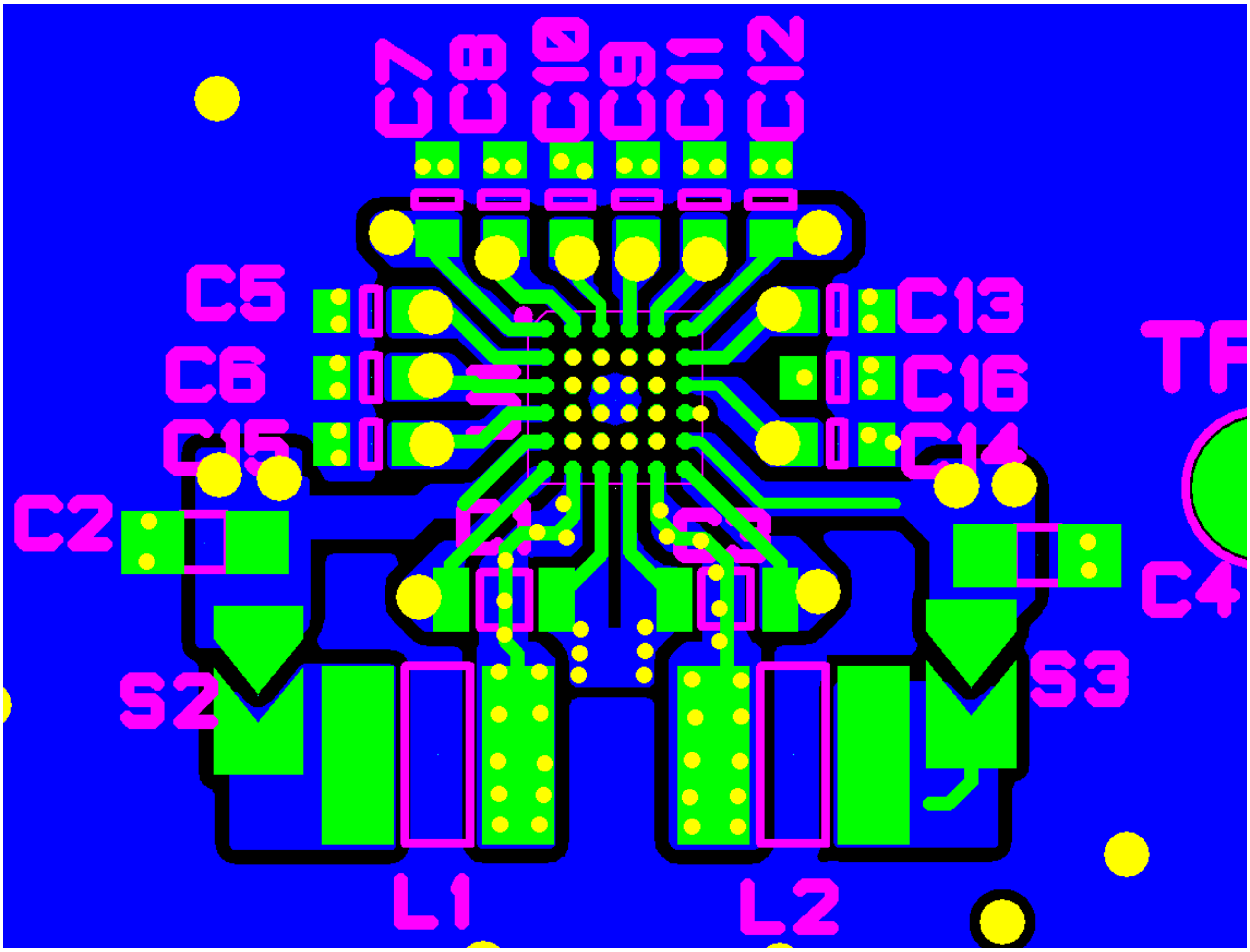


Figure 48. Demoboard Example

THERMAL CONSIDERATIONS

Careful attention must be paid to the power dissipation of the NCP6925. The power dissipation is a function of efficiency and output power. Hence, increasing the output power requires better components selection. Care should be taken of LDO V_{DROP}, the larger it is, the higher dissipation it will bring to NCP6925. Keep a large copper plane under and close to NCP6925 is helpful for thermal dissipation.

ORDERING INFORMATION

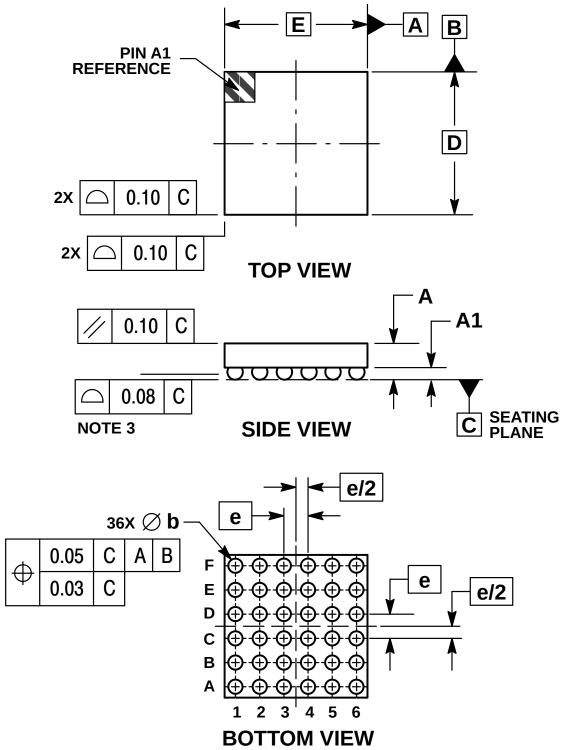
Device	Marking	Package	Shipping†	Comment
NCP6925AFCT1G (*)	6925A	WLCSP30 − 2.36 x 2.36 mm (Pb−Free)	3,000 / Tape & Reel	(see detailed description)
NCP6925AFCT2G (*)	6925A	WLCSP30 − 2.36 x 2.36 mm (Pb−Free)	3,000 / Tape & Reel	(see detailed description)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This is flip chip package without die coating

Demo Board Available:
The NCP6925GEVB/D evaluation board configures the device in typical application to supply constant voltage.

PACKAGE DIMENSIONS

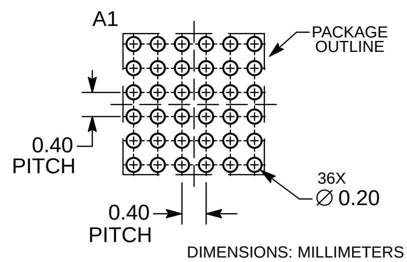
WLCSP36 2.36x2.36
CASE 567GW
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.17	0.23
b	0.24	0.29
D	2.36 BSC	
E	2.36 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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For additional information, please contact your local Sales Representative